Summer School on Information Engineering

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Trends and Challenges in VLSI Technology Scaling

G. Baccarani

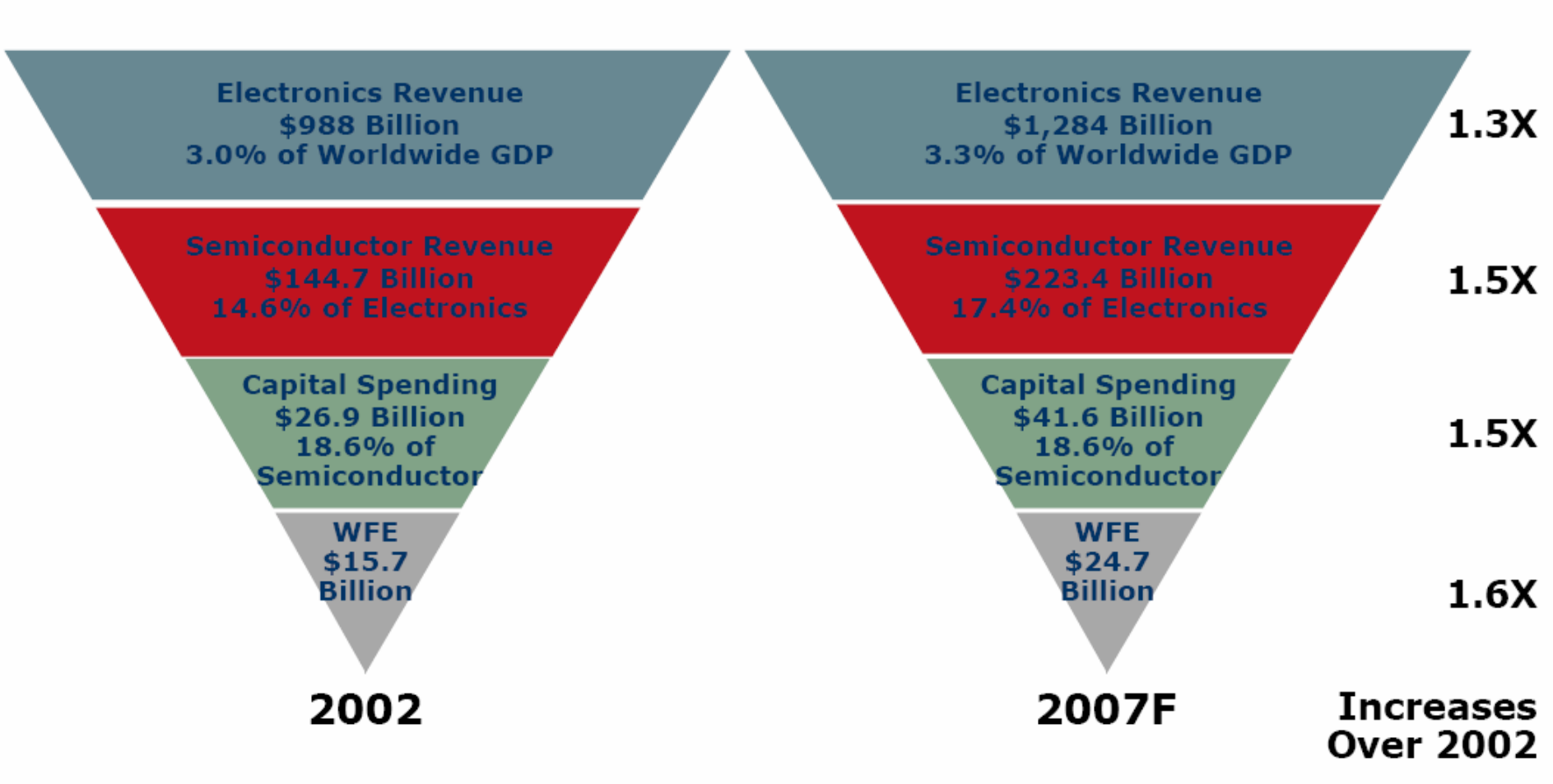
Advanced Research Center on Electronic Systems (ARCES),
Department of Electronics (DEIS) – University of Bologna, Italy

Arces
University of Bologna

Outline

- Evolution from micro- to nano-electronics
- Device miniaturization and scaling theory
- The ITRS and its impact on the research area
- Evolution of interconnects and packaging
- Functional requirements of CMOS logic gates
- New device architectures
- Device modeling issues
- Conclusions

Size of the Electronic Market



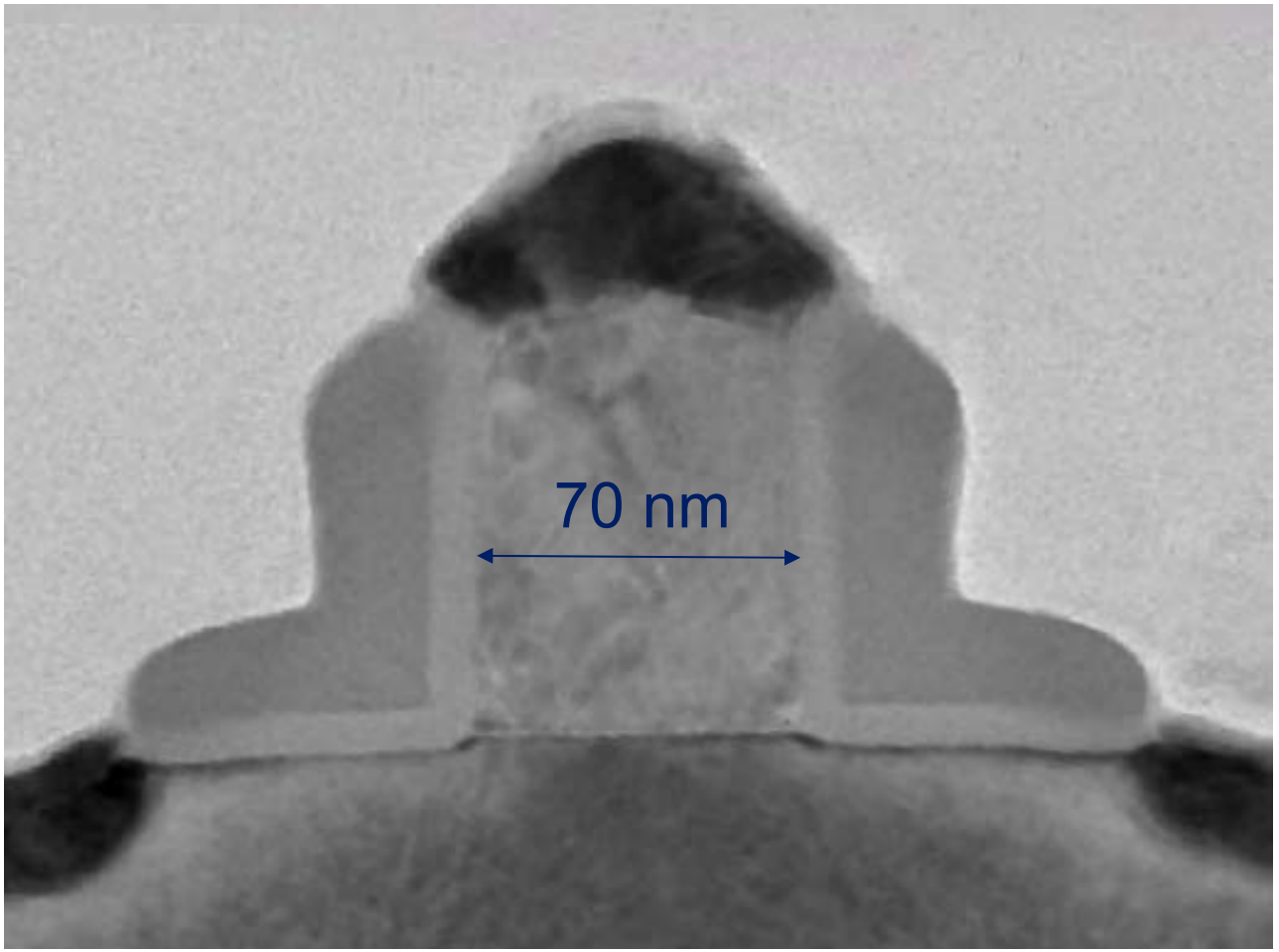
Sources: Dataquest, Applied Materials, WSTS, SEMI

Definition of Nanotechnology

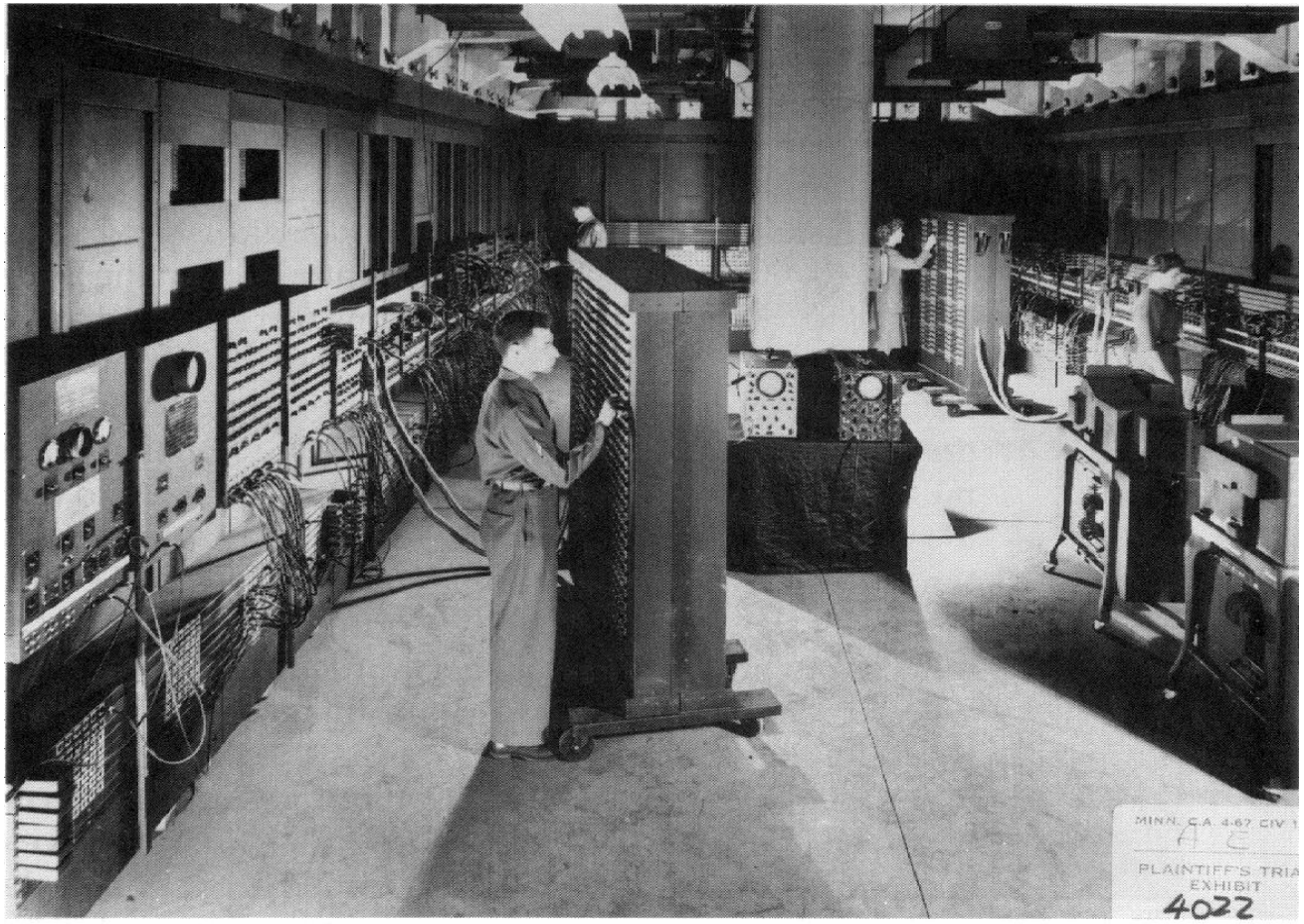
- Working at the length scale of 1-100 nm to create materials, devices, and systems with fundamentally new properties and functions because of their nanoscale size.

from www.nano.gov

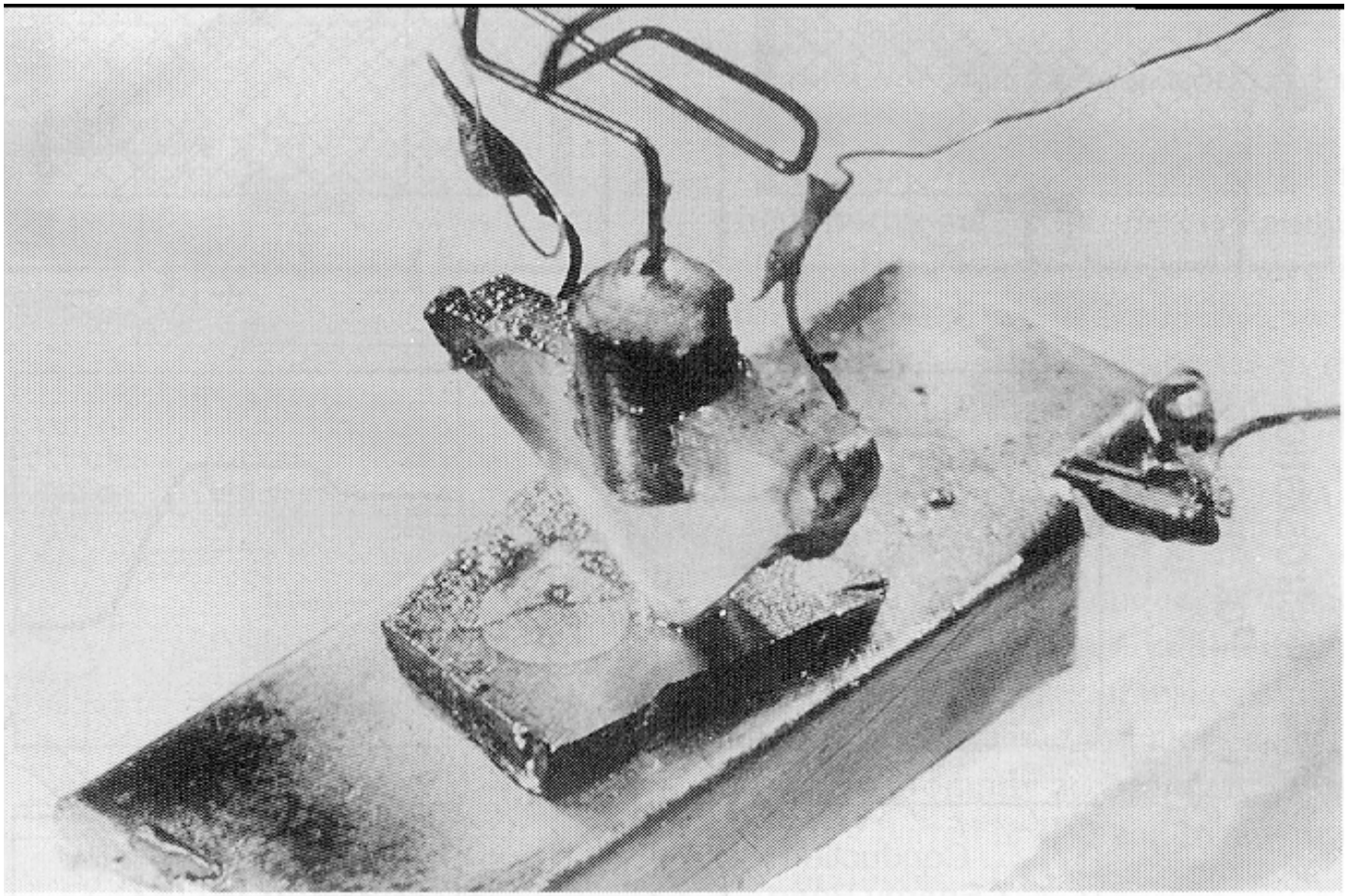
70 nm Gate Length FET



ENIAC - the First Electronic Computer (1946)



The First Transistor (1948)



First transistor
Bell Labs, 1948

The Transistor Revolution (1948)

The Nobel Prize in Physics 1956

"for their researches on semiconductors and their discovery of the transistor effect"

William B. Shockley

John Bardeen

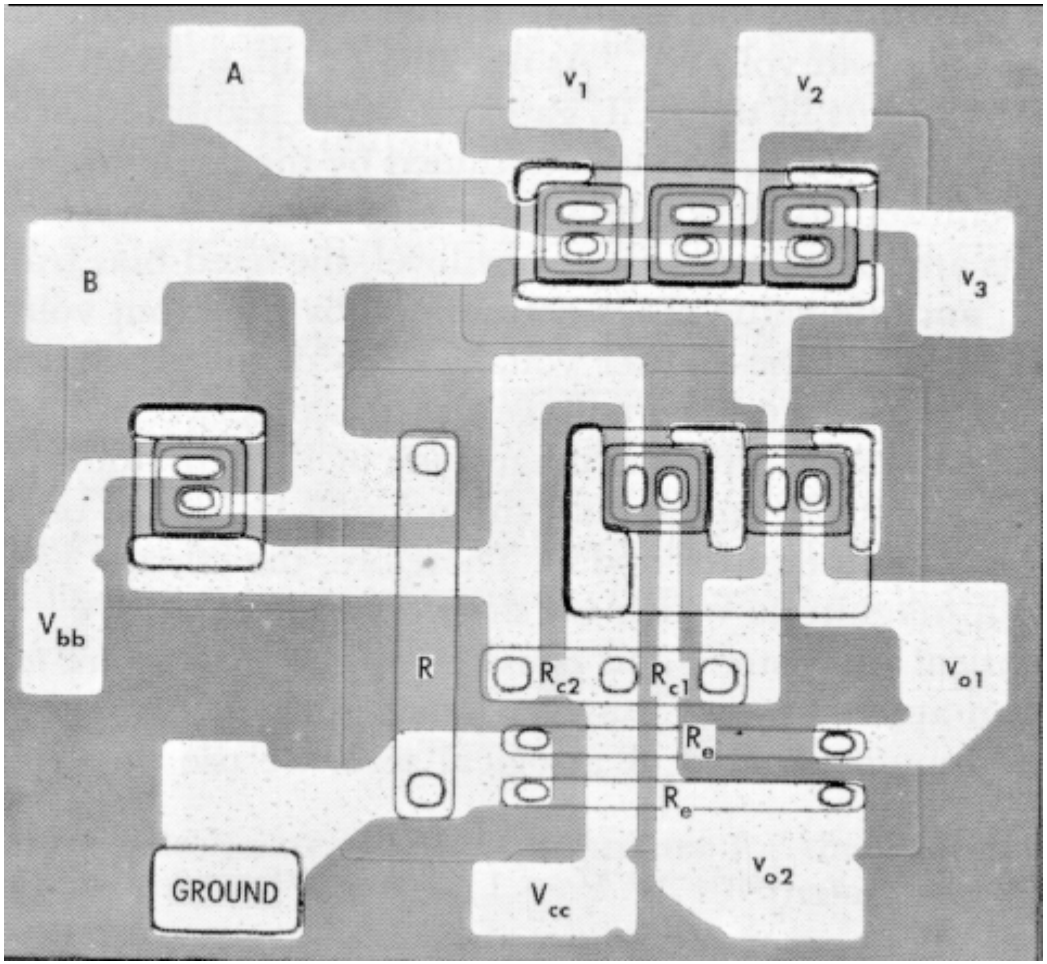
Walter H. Brattain

The First Integrated Circuit (1961)

J. Kilby:
Two transistors laid out onto the same semiconductor substrate and connected by external wiring

R. Noyce:
Two transistors laid out onto the same semiconductor substrate and connected by on-chip metallization

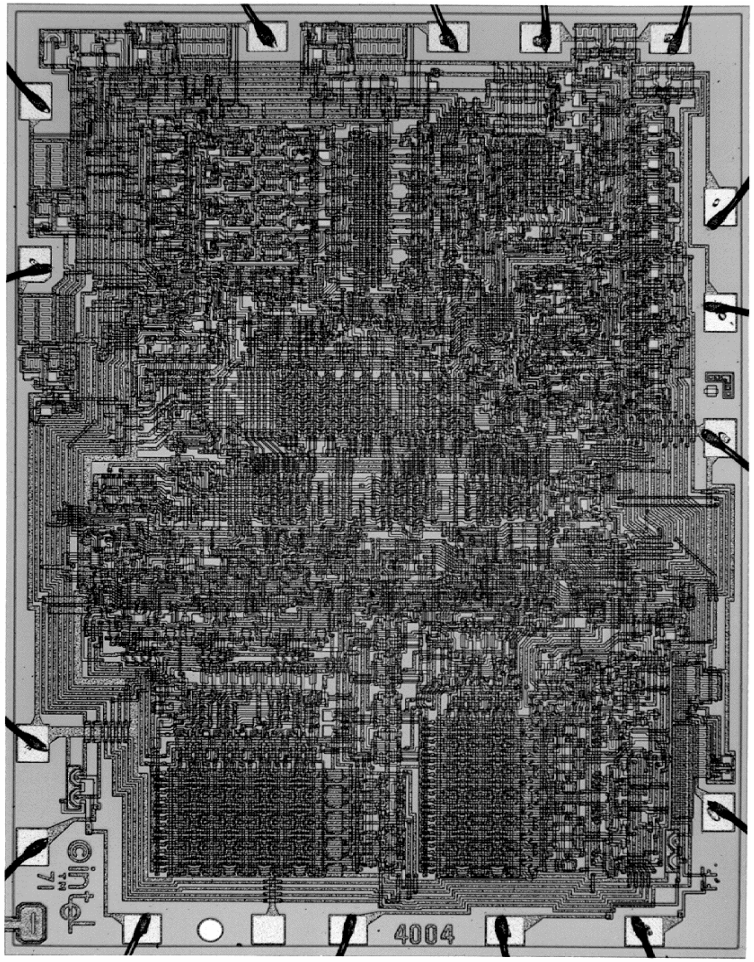
The First Commercial Integrated Circuit (1966)



Bipolar logic
1960's

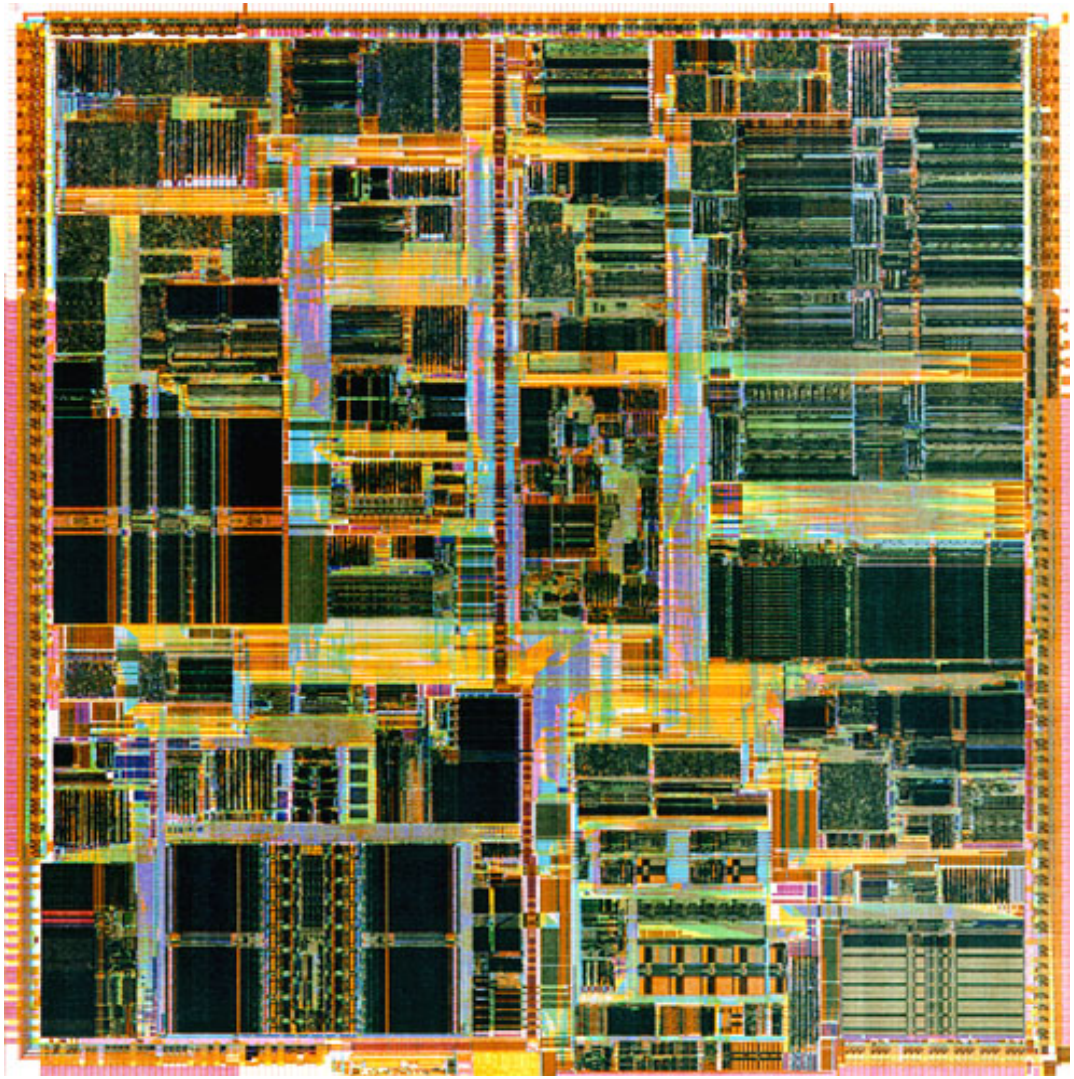
ECL 3-input Gate
Motorola 1966

The First Microprocessor (1971)



INTEL 4004
Microprocessor (1971)
M. Huff – F. Faggin
1000 transistors
1 MHz operation

INTEL Pentium IV Microprocessor

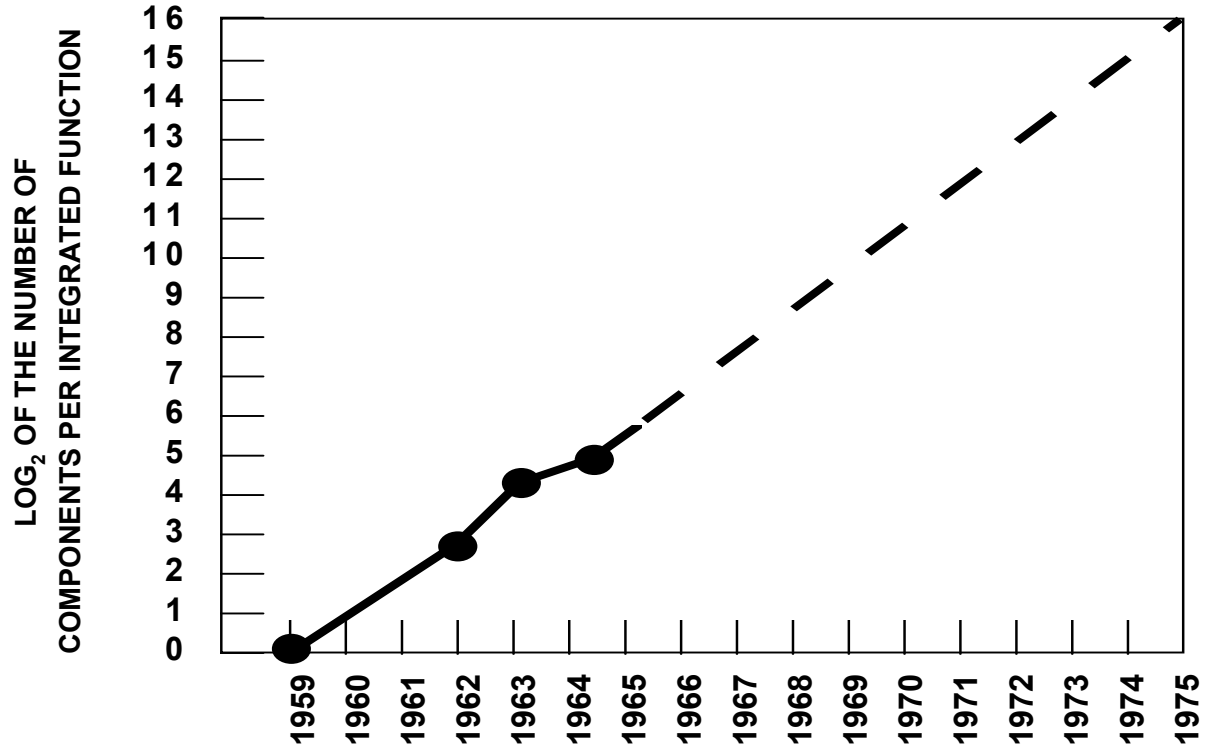


INTEL Pentium IV Microprocessor
42 Million Transistors

Moore's Law (1964)

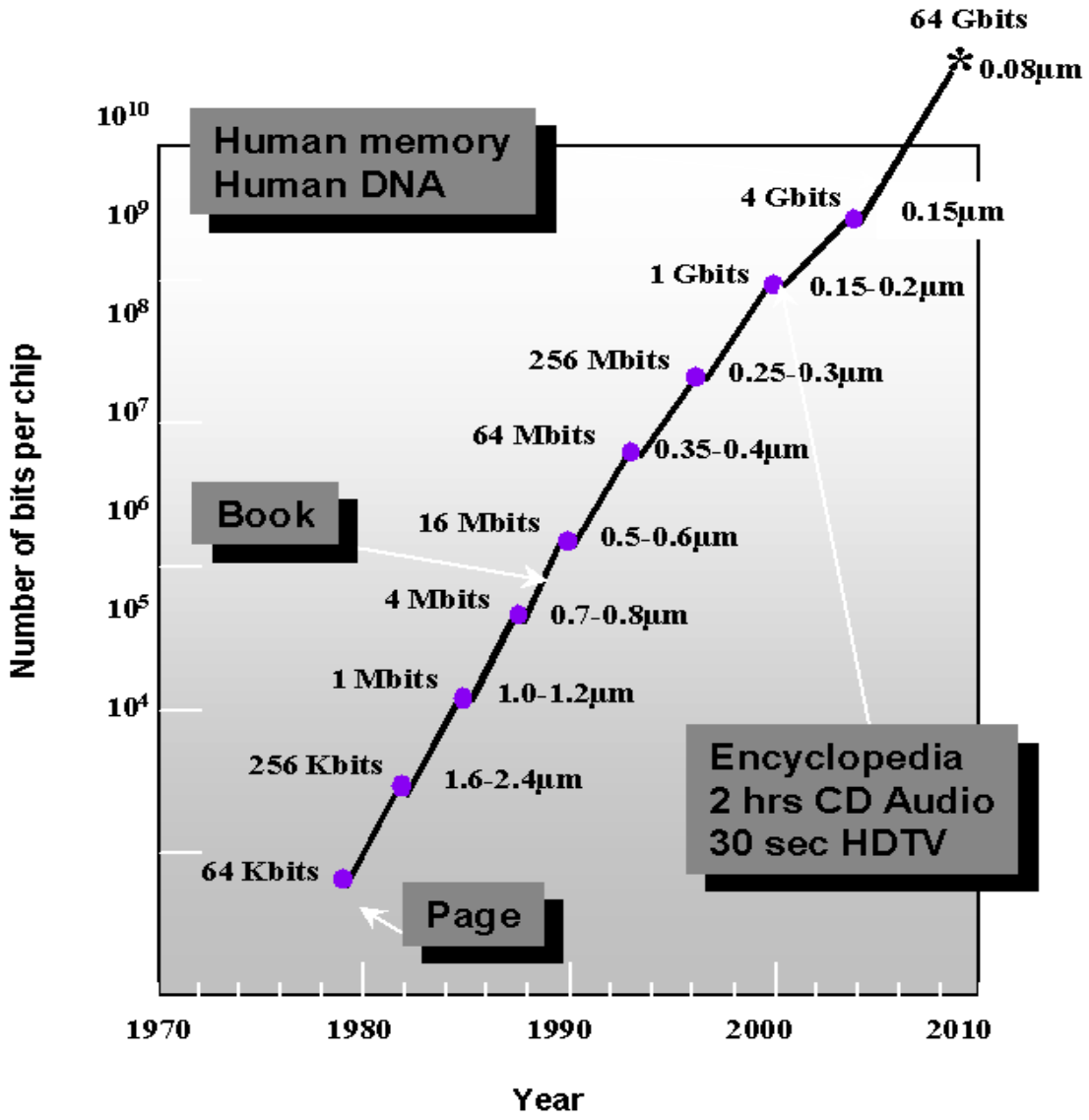
- In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 18 to 24 months.
- He made a prediction that semiconductor technology would double its effectiveness every 18 months

Moore's Law



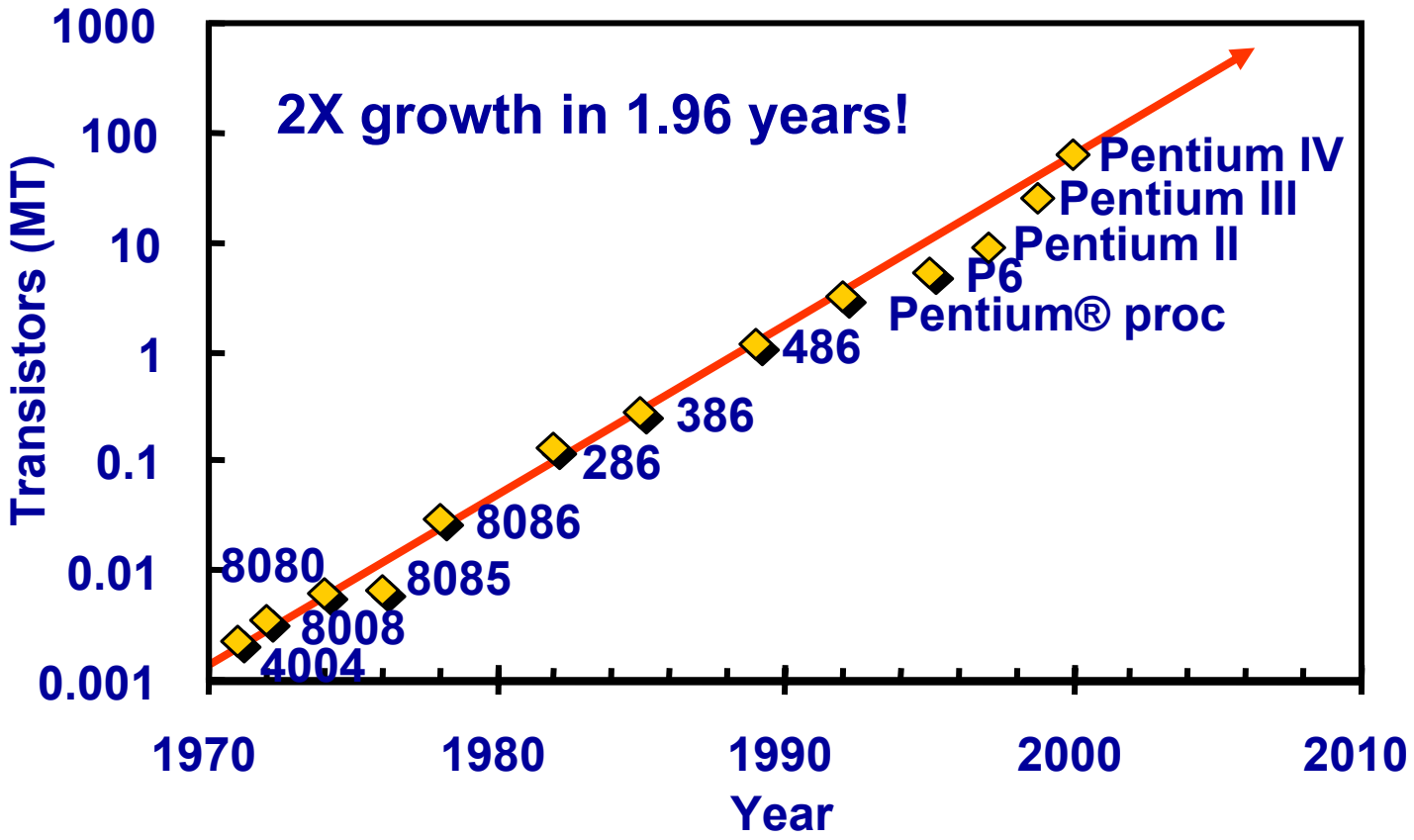
Electronics, April 19, 1965.

Evolution of Complexity

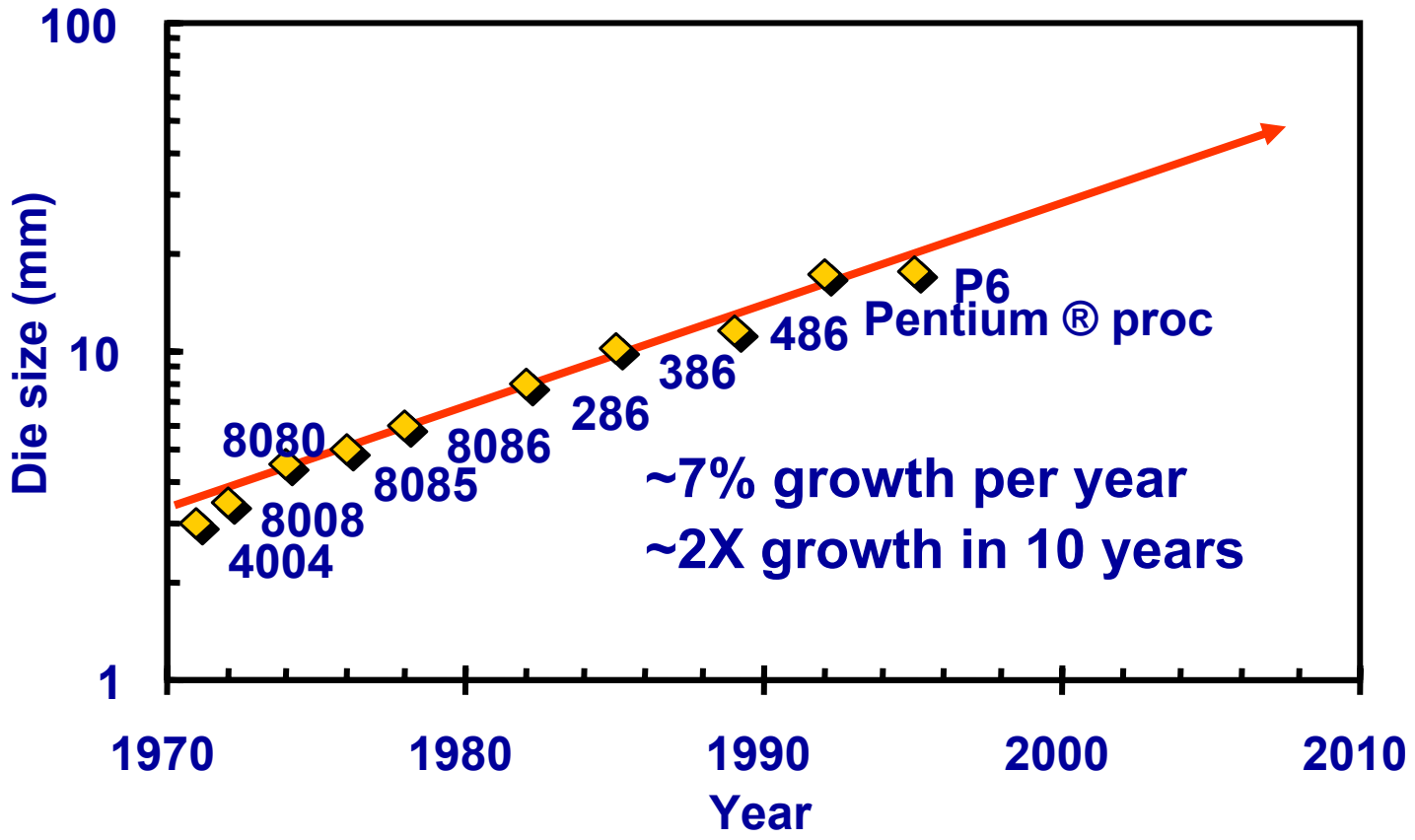


Moore's Law for Microprocessors

Transistors on Lead Microprocessors double every 2 years



Die Size Growth



Die size grows by 7% per year to satisfy Moore's Law

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Why Scaling?

- Technology shrinks by 0.7/generation
- With every generation we can integrate 2x more functions per chip; chip cost does not increase significantly
- Cost of a function decreases by 2x
- But …
  - How to design chips with more and more functions?
  - Design engineering population does not double every two years…
- Hence, a need for more efficient design methods
  - Exploit different levels of abstraction

Technology Scaling Models

- Full Scaling (constant electric field)

  Dimensions and voltages scale together by the same factor λ

- Fixed Voltage Scaling

  Only dimensions scale; voltages remain constant

- General Scaling

  Voltages and dimensions scale by different and independent factors

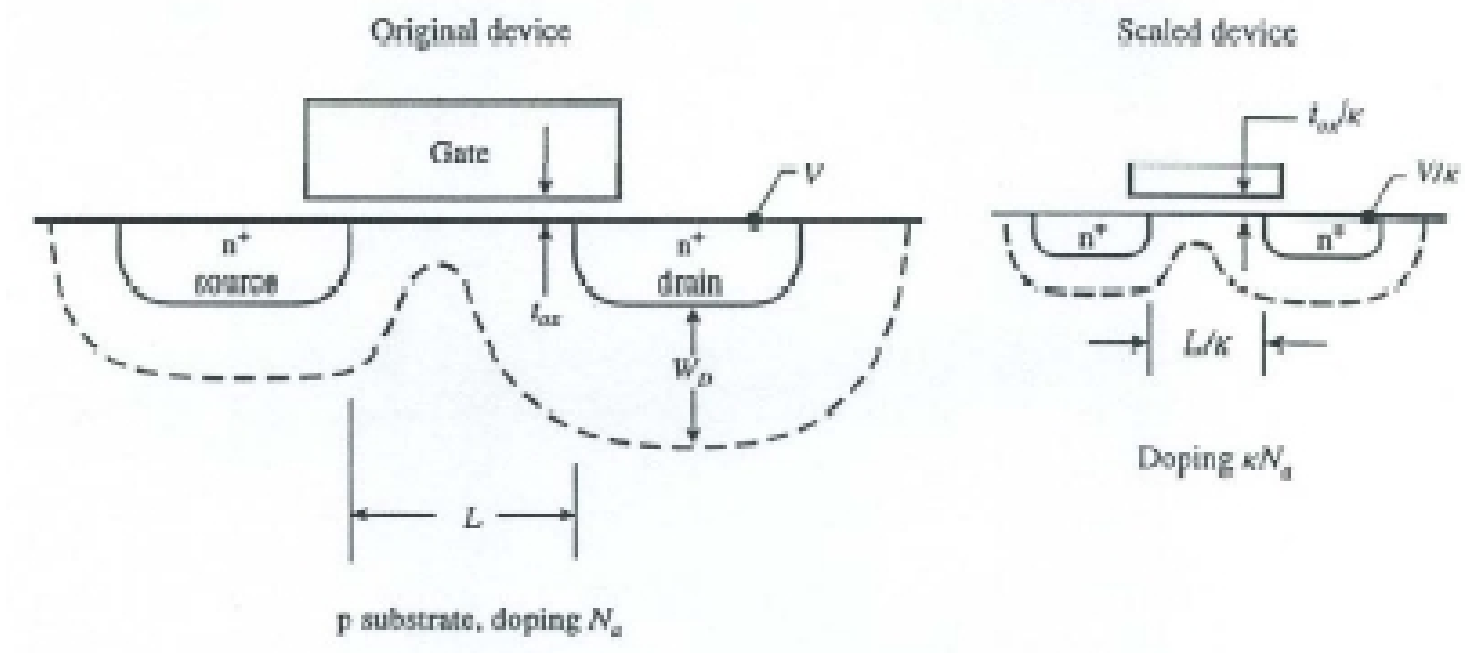
Constant Field Scaling (Long-channel FETs)

Phys. Parameters	Expressions	Scaling factor
Dimensions	W, L, t_{ox}, x_j	$1/\lambda$
Voltages	V_{GS}, V_{DS}	$1/\lambda$
Impurity Conc.	N_A, N_D	λ
Electric Field	E	1
Current	$(W/2L)\,\mu C_{ox}\,(V_{GS} - V_T)^2$	$1/\lambda$
Transconductance	$(W/L)\,\mu C_{ox}\,(V_{GS} - V_T)$	1
Gate Delay	$C_L V_{DD}/I_D$	$1/\lambda$
Power	$I_D V_{DD}$	$1/\lambda^2$
Power-Delay Pr.	$C_L V_{DD}^2$	$1/\lambda^3$
Power density	P_d/A_{gate}	1
Current density	I_D/A_{int}	λ

Constant-Field Scaling (Short-Channel FETs)

Phys. Parameters	Expressions	Scaling factor
Dimensions	W, L, t_{ox}, x_j	$1/\lambda$
Voltages	V_{GS}, V_{DS}	$1/\lambda$
Impurity Conc.	N_A, N_D	λ
Electric Field	E	1
Current	$W\,C_{ox}\,(V_{GS} - V_T)v_{sat}$	$1/\lambda$
Transconductance	$W\,C_{ox}\,v_{sat}$	1
Gate Delay	$C_L V_{DD}/I_D$	$1/\lambda$
Power	$I_D V_{DD}$	$1/\lambda^2$
Power-Delay Pr.	$C_L V_{DD}^2$	$1/\lambda^3$
Power density	P_d/A_{gate}	1
Current density	I_D/A_{int}	λ

Constant-Field Scaling (Short-Channel FETs)



(R.H. Dennard, IBM, 1978)

Fixed-Voltage Scaling (Long-Channel FETs)

Phys. Parameters	Expressions	Scaling factor
Dimensions	W, L, t_{ox}, x_j	$1/\lambda$
Voltages	V_{GS}, V_{DS}	1
Impurity Conc.	N_A, N_D	λ^2
Electric Field	E	λ
Current	$(W/2L)\mu C_{ox}(V_{GS} - V_T)^2$	λ
Transconductance	$(W/L)\,\mu C_{ox}\,(V_{GS} - V_T)$	λ
Gate Delay	$C_L V_{DD}/I_D$	$1/\lambda^2$
Power	$I_D V_{DD}$	λ
Power-Delay Pr.	$C_L V_{DD}^2$	$1/\lambda$
Power density	P_d/A_{gate}	λ^3
Current density	I_D/A_{int}	λ^3

Fixed Voltage Scaling (Short-Channel FETs)

Phys. Parameters	Expressions	Scaling factor
Dimensions	W, L, t_{ox}, x_j	$1/\lambda$
Voltages	V_{GS}, V_{DS}	1
Impurity Conc.	N_A, N_D	λ^2
Electric Field	E	λ
Current	$W\, C_{ox}\, (V_{GS} - V_T) v_{sat}$	1
Transconductance	$W\, C_{ox}\, v_{sat}$	1
Gate Delay	$C_L V_{DD}/I_D$	$1/\lambda$
Power	$I_D V_{DD}$	1
Power-Delay Pr.	$C_L V_{DD}^2$	$1/\lambda$
Power density	P_d/A_{gate}	λ^2
Current density	I_D/A_{int}	λ^2

Generalized Scaling Theory

$$\frac{\partial^2 \Phi}{\partial X^2} + \frac{\partial^2 \Phi}{\partial Y^2} + \frac{\partial^2 \Phi}{\partial Z^2} = -\frac{q}{\varepsilon}\left(P - N + N_D - N_A\right)$$

$$\phi = \Phi/\kappa \qquad (x, y, z) = (X, Y, Z)/\lambda$$

$$(p, n, n_D, n_A) = (P, N, N_D, N_A)\,\lambda^2/\kappa$$

$$\frac{\partial^2(\kappa\phi)}{\partial(\lambda x)^2} + \frac{\partial^2(\kappa\phi)}{\partial(\lambda y)^2} + \frac{\partial^2(\kappa\phi)}{\partial(\lambda z)^2} = -\frac{q}{\varepsilon}\left(p - n + n_D - n_A\right)\kappa/\lambda^2$$

$$\frac{\partial^2 \phi}{\partial x^2} + \frac{\partial^2 \phi}{\partial y^2} + \frac{\partial^2 \phi}{\partial z^2} = -\frac{q}{\varepsilon}\left(p - n + n_D - n_A\right)$$

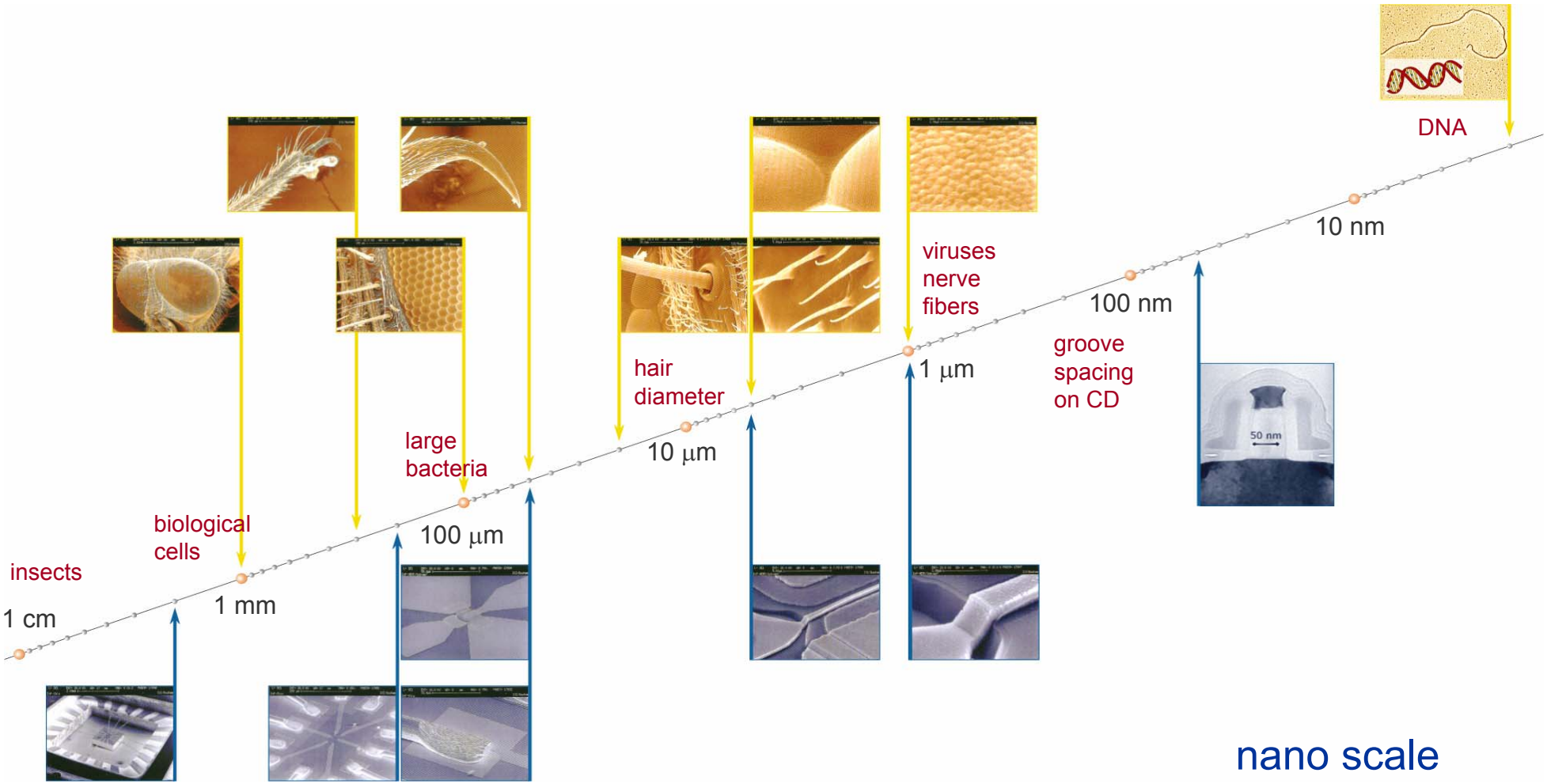
Scaling Relationships (Long-Channel FETs)

Phys. Parameters	Expressions	Scaling factor
Dimensions	W, L, t_{ox}, x_j	$1/\lambda$
Voltages	V_{GS}, V_{DS}	$1/\kappa$
Impurity Conc.	N_A, N_D	λ^2/κ
Electric Field	E	λ/κ
Current	$(W/2L)\,\mu C_{ox}\,(V_{GS}-V_T)^2$	λ/κ^2
Transconductance	$(W/L)\,\mu C_{ox}\,(V_{GS}-V_T)$	λ/κ
Gate Delay	$C_L V_{DD}/I_D$	κ/λ^2
Power	$I_D V_{DD}$	λ/κ^3
Power-Delay Pr.	$C_L V_{DD}^2$	$1/\lambda\kappa^2$
Power density	P_d/A_{gate}	λ^3/κ^3
Current density	I_D/A_{int}	λ^3/κ^2

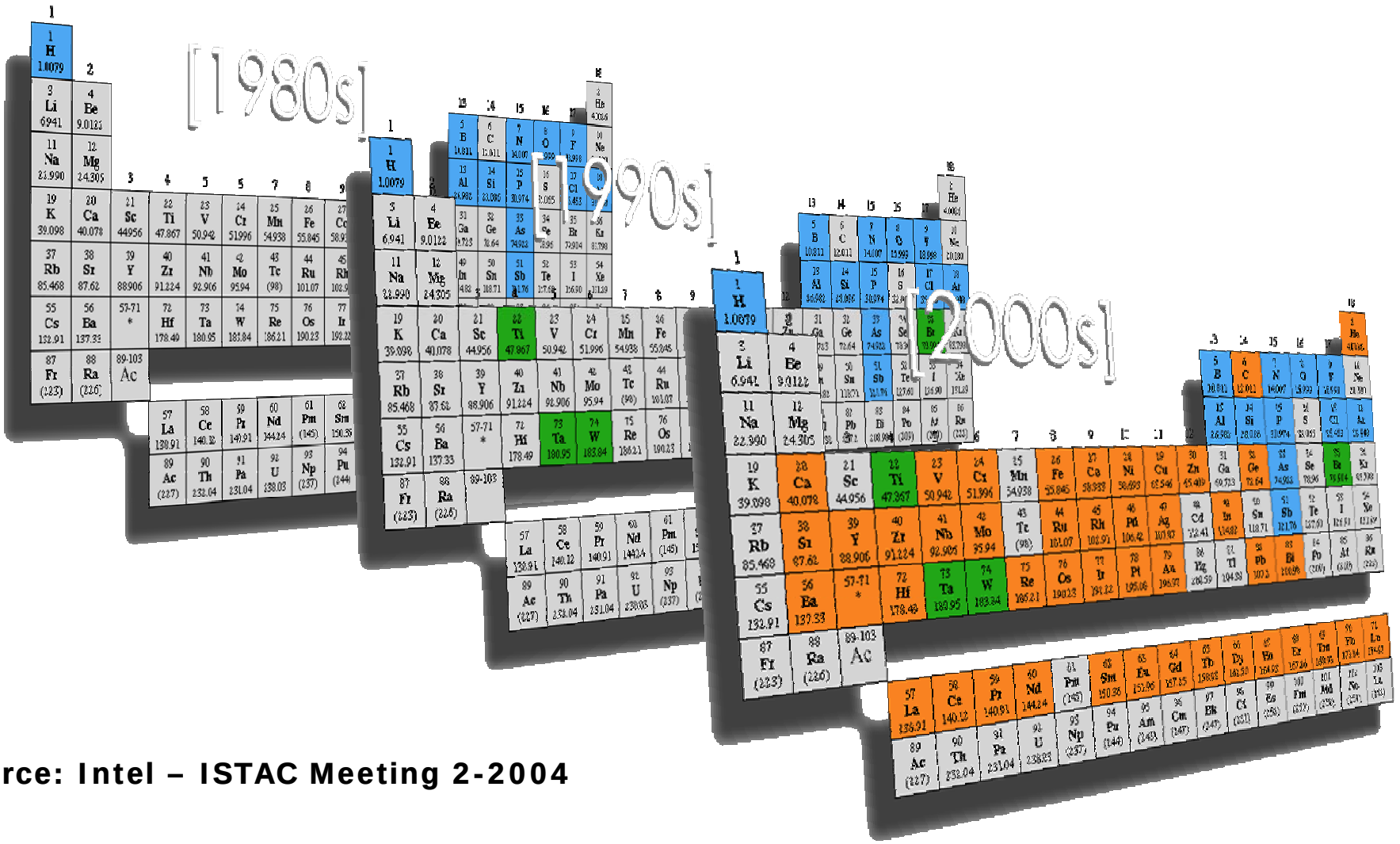
Scaling Relationships (Short-Channel FETs)

Phys. Parameters	Expressions	Scaling factor
Dimensions	W, L, t_{ox}, x_j	$1/\lambda$
Voltages	V_{GS}, V_{DS}	$1/\kappa$
Impurity Conc.	N_A, N_D	λ^2/κ
Electric Field	E	λ/κ
Current	$W\,C_{ox}\,(V_{GS} - V_T)v_{sat}$	$1/\kappa$
Transconductance	$W\,C_{ox}\,v_{sat}$	1
Gate Delay	$C_L V_{DD}/I_D$	$1/\lambda$
Power	$I_D V_{DD}$	$1/\kappa^2$
Power-Delay Pr.	$C_L V_{DD}^2$	$1/\lambda\kappa^2$
Power density	P_d/A_{gate}	λ^2/κ^2
Current density	I_D/A_{int}	λ^2/κ

Feature size scaling

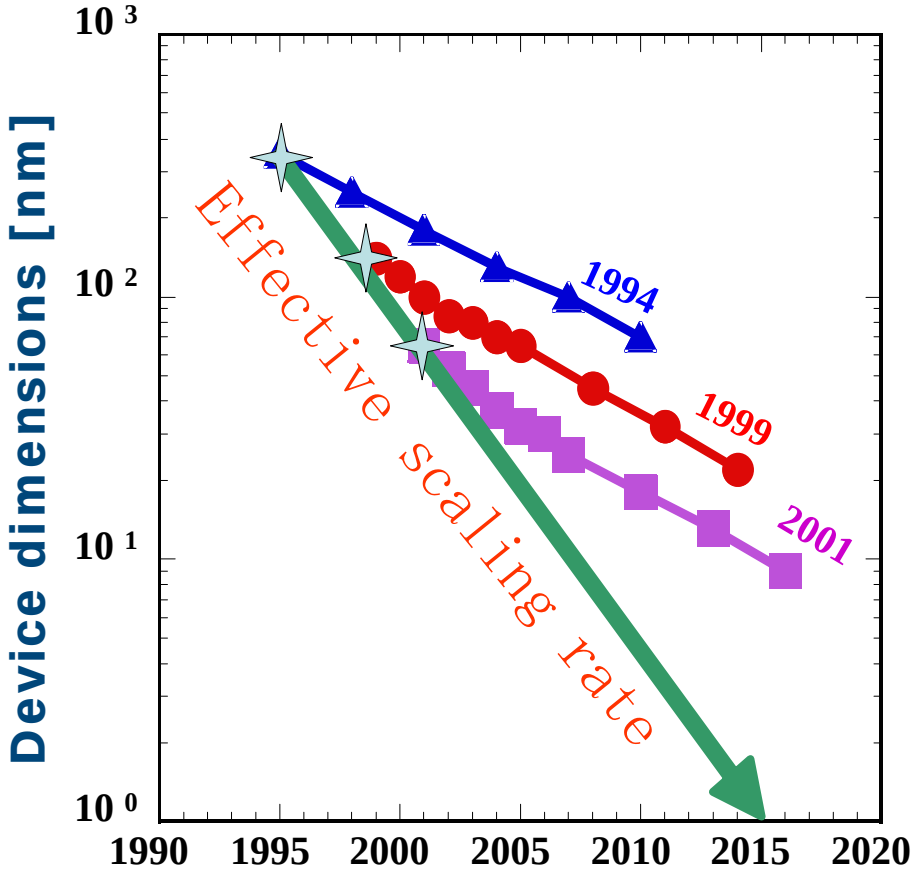


Si technology: complexity increasing exponentially



Source: Intel – ISTAC Meeting 2-2004

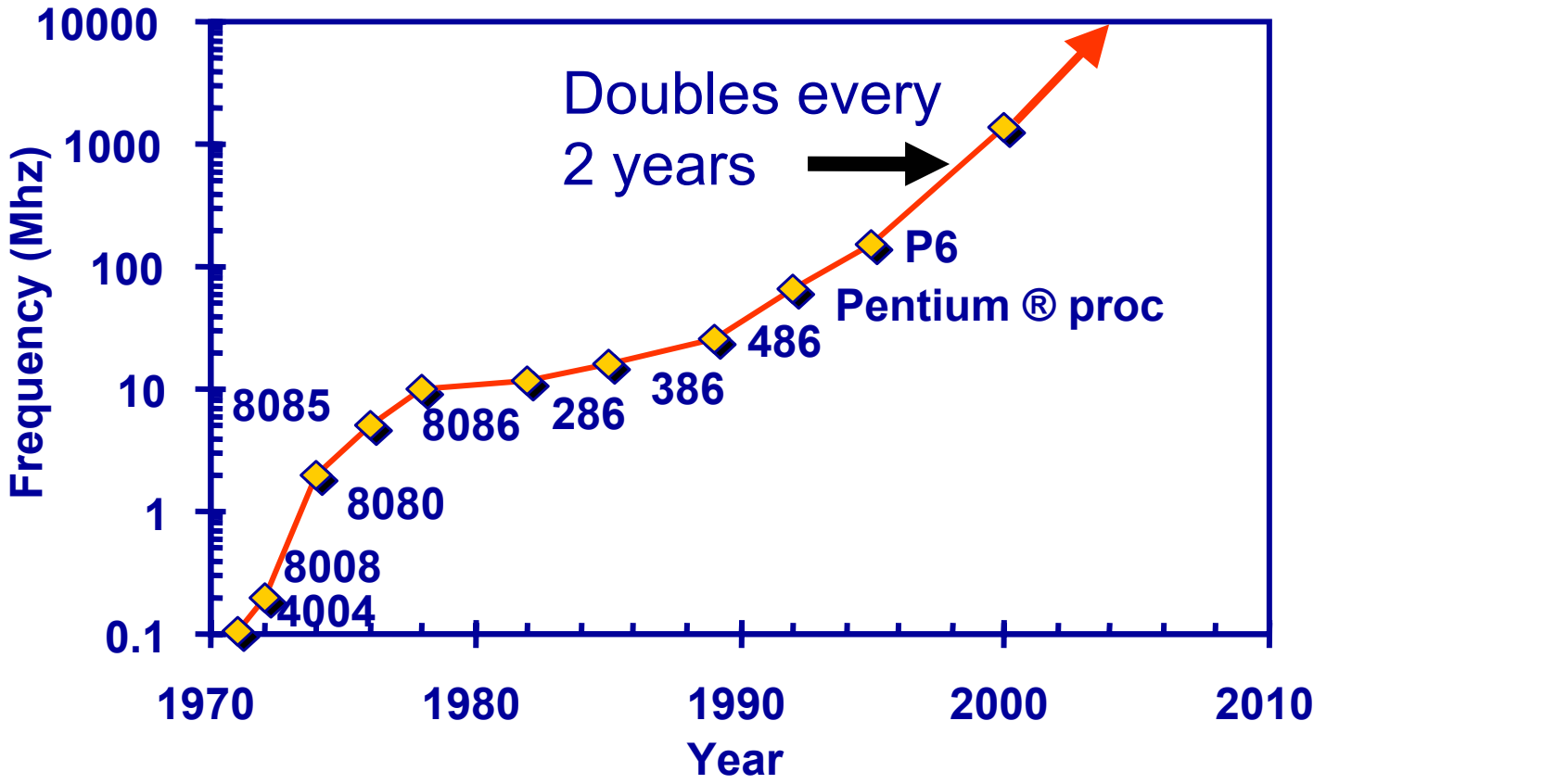
Complexity and acceleration



Boron
Phosphorous
Aluminum
SiO2
Silicon
1970

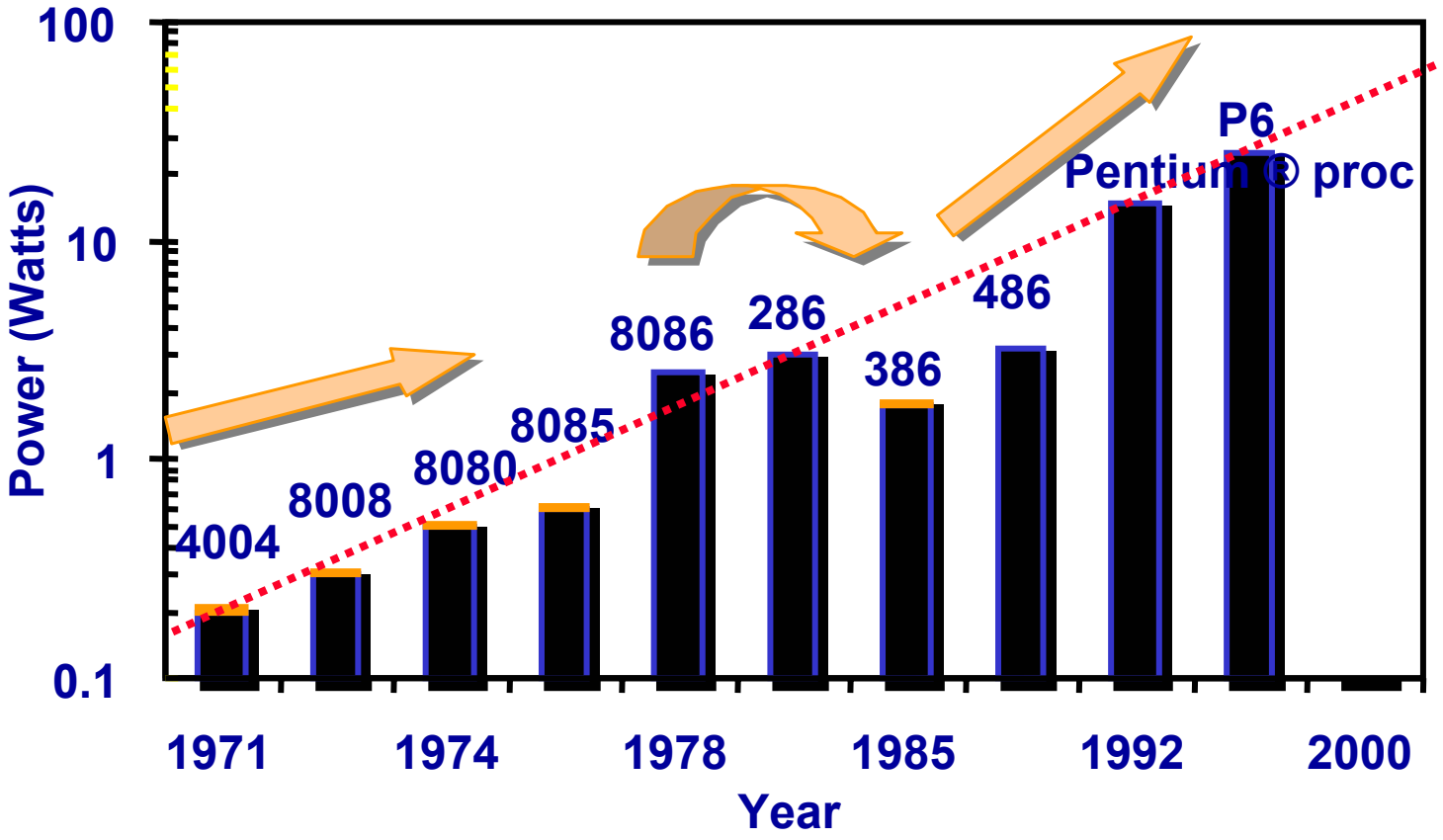
Silicon-Germanium
Metal gates
High-k dielectrics
Low-k dielectrics
Copper interconnects
Tungsten plugs
Cobalt silicide
Titanium silicide
Nichel silicide
BPSG
Polysilicon
Silicon nitride
Oxinitrides
Indium
Arsenic
Boron
Phosphorous
Aluminum
SiO2
Silicon
2000

Clock Frequency



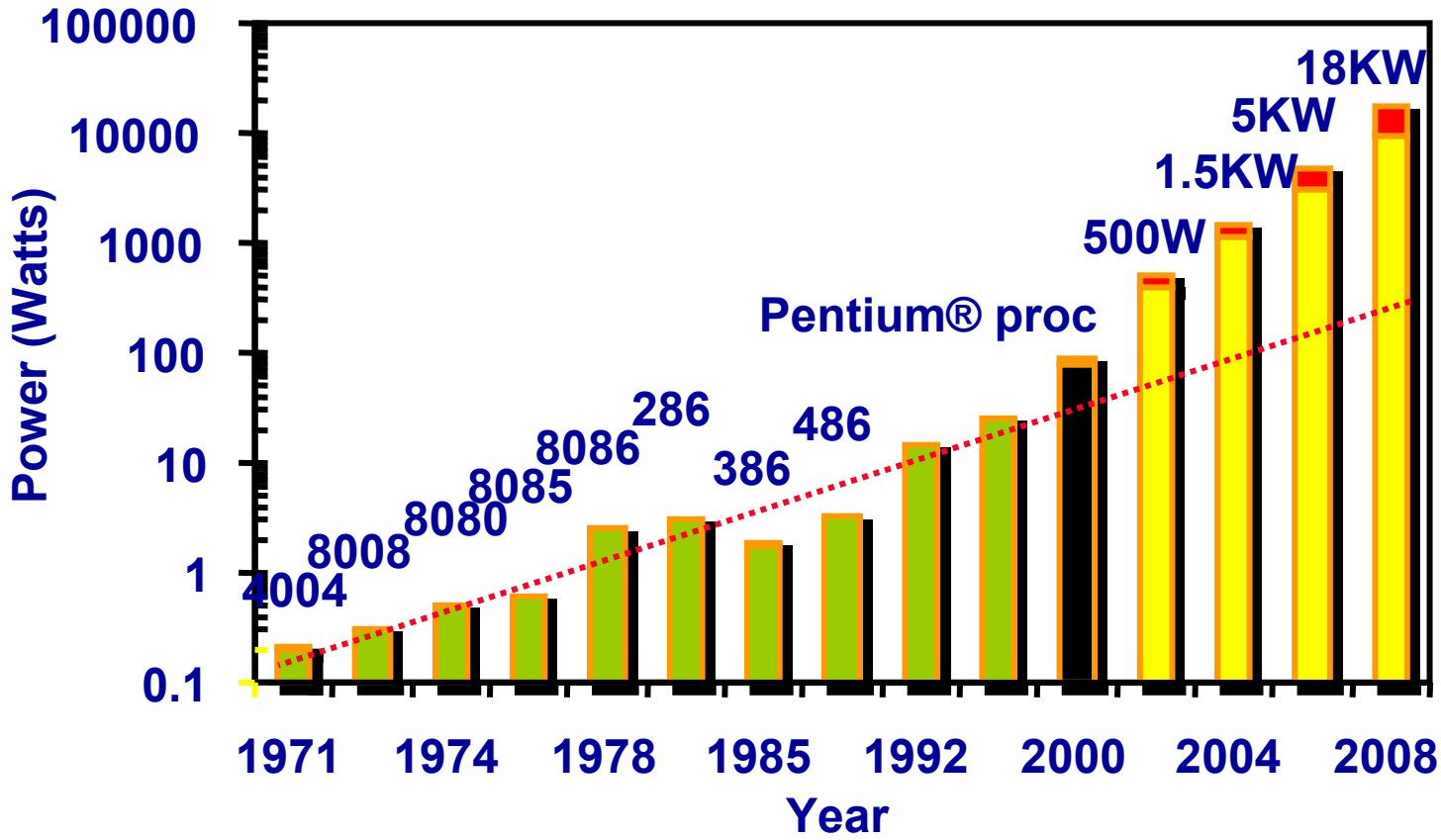
Lead Microprocessors frequency doubles every 2 years

Power Dissipation



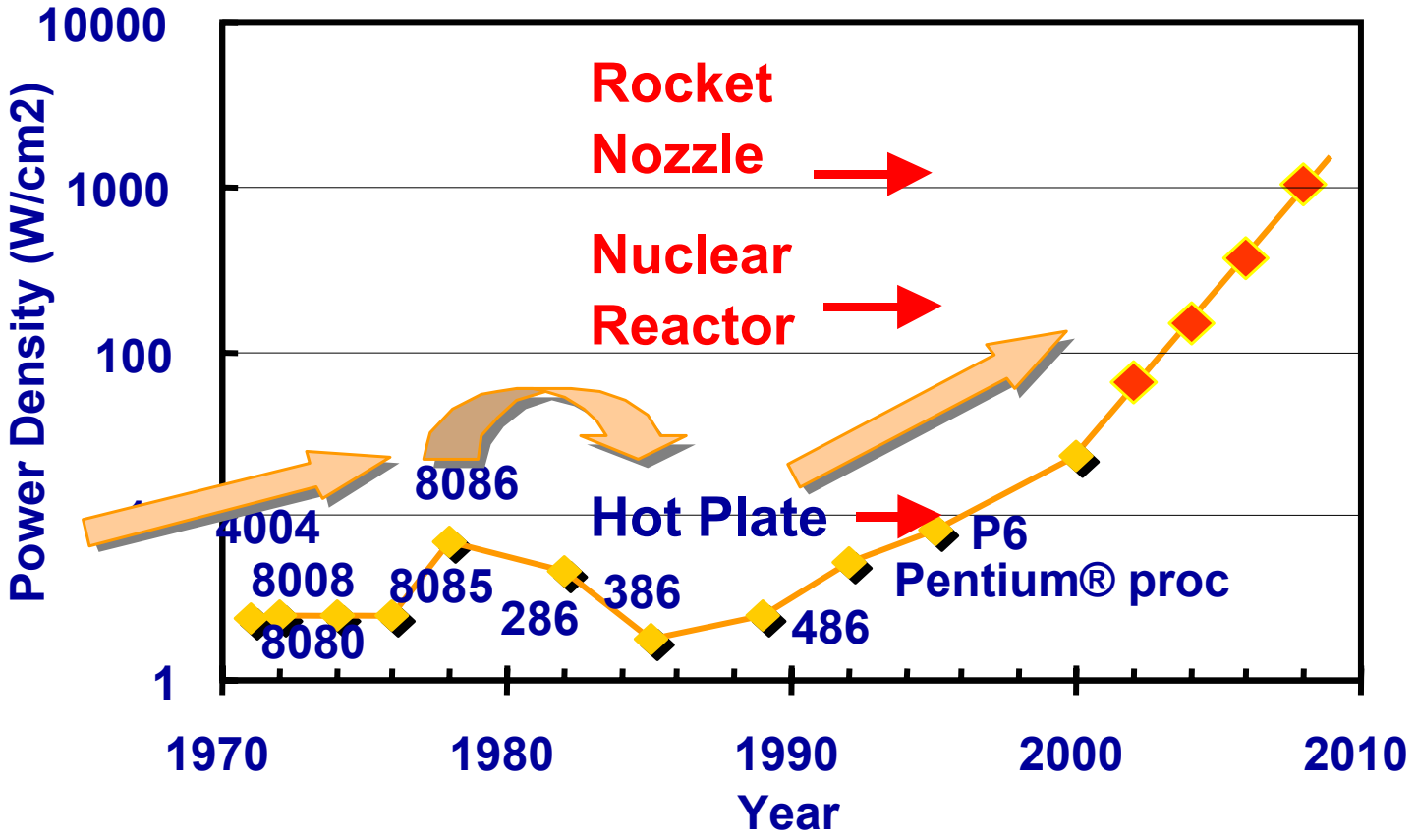
Lead Microprocessors power continues to increase

Power Dissipation Trend



Power delivery and dissipation will be prohibitive

Power Density



Power density too high to keep junctions at low temp

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ITRS Technology Nodes

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
L_g: Physical L_{gate} for High Performance logic (nm) [1]	**32**	**28**	**25**	**22**	**20**	**18**	**16**	**14**	**13**
EOT: Equivalent Oxide Thickness [2]									
Extended planar bulk (Å)	**12**	**11**	**11**	**9**	**7.5**	**6.5**	**5**	**5**	
UTB FD (Å)				**9**	**8**	**7**	**6**	**5**	**5**
DG (Å)							**8**	**7**	**6**
Gate Poly Depletion and Inversion-Layer Thickness [3]									
Extended Planar Bulk (Å)	**7.3**	**7.4**	**7.4**	**2.9**	**2.8**	**2.7**	**2.5**	**2.5**	
UTB FD (Å)				**4**	**4**	**4**	**4**	**4**	**4**
DG (Å)							**4**	**4**	**4**
EOT_{elec}: Electrical Equivalent Oxide Thickness in inversion [4]									
Extended Planar Bulk (Å)	**19.3**	**18.4**	**18.4**	**11.9**	**10.3**	**9.2**	**7.5**	**7.5**	
UTB FD (Å)				**13**	**12**	**11**	**10**	**9**	**9**
DG (Å)							**12**	**11**	**10**

ITRS Technology Nodes

V_{dd}: Power Supply Voltage (V) [6]	1.1	1.1	1.1	1	1	1	1	0.9	0.9
$V_{t,sat}$: Saturation Threshold Voltage [7]									
Extended Planar Bulk (mV)	195	168	165	160	159	151	146	148	
UTB FD (mV)				169	168	167	170	166	167
DG (mV)							181	184	185
$I_{sd,leak}$: Source/Drain Subthreshold Off-State Leakage Current [8]									
Extended Planar Bulk (μA/μm)	0.06	0.15	0.2	0.2	0.22	0.28	0.32	0.34	
UTB FD (μA/μm)				0.17	0.19	0.22	0.22	0.29	0.29
DG (μA/μm)							0.1	0.11	0.11
$I_{d,sat}$: effective NMOS Drive Current [9]									
Extended Planar Bulk (μA/μm)	1020	1130	1200	1570	1810	2050	2490	2300	
UTB FD (μA/μm)				1486	1625	1815	2015	2037	2198
DG (μA/μm)							1899	1932	2220
Mobility Enhancement Factor for $I_{d,sat}$ [10]									
Extended Planar Bulk	1.09	1.09	1.08	1.09	1.10	1.10	1.12	1.11	
UTB FD				1.06	1.06	1.06	1.06	1.05	1.05
DG							1.05	1.04	1.05
Effective Ballistic Enhancement Factor [11]									
Extended Planar Bulk	1	1	1	1	1	1	1	1	
UTB FD				1	1	1	1	1	1.1
DG							1.17	1.25	1.31

CMOS Outlook

High Volume Manufacturing	2004	2006	2008	2010	2012	2014	2016	2018
Technology Node (nm)	90	65	45	32	22	16	11	8
Integration Capacity (BT)	2	4	8	16	32	64	128	256
Delay = CV/I scaling	0.7	~0.7	>0.7	Delay scaling will slow down				
Energy/Logic Op scaling	>0.35	>0.5	>0.5	Energy scaling will slow down				
Bulk Planar CMOS	High Probability					Low Probability		
Alternate, 3G etc	Low Probability					High Probability		
Variability	Medium			High		Very High		
ILD (K)	~3	<3	Reduce slowly towards 2-2.5					
RC Delay	1	1	1	1	1	1	1	1
Metal Layers	6-7	7-8	8-9	0.5 to 1 layer per generation				

Scaling Roadblocks

- Reduced line width → EUV lithography (13 nm)
- Tunneling through the gate oxide → high-κ dielectrics
- Poly gate depletion capacitance → metal gate
- Propagation delay (RC) through long-distance interconnects → low-κ dielectrics
- Threshold voltage scaling and increased leakage current
- Increased power dissipation per unit area

Scaling Roadblocks

- Increased drain-induced barrier lowering (DIBL)
- Reduced subthreshold slope (SS)
- Increased threshold-voltage roll-off
- Increased gate-induced drain leakage (GIDL)
- Increased statistical fluctuations of the threshold voltage due to randomness of the dopant atoms
- Solution: new device architectures

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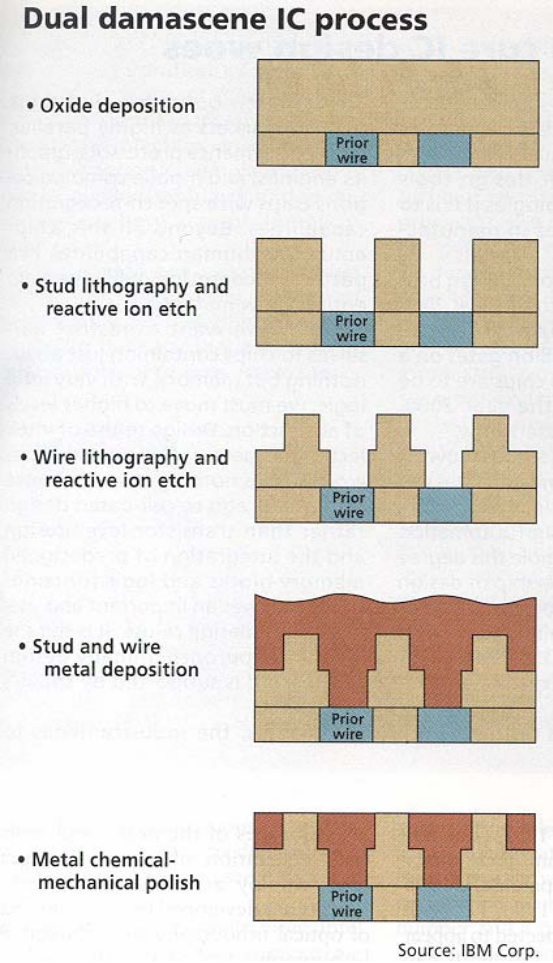
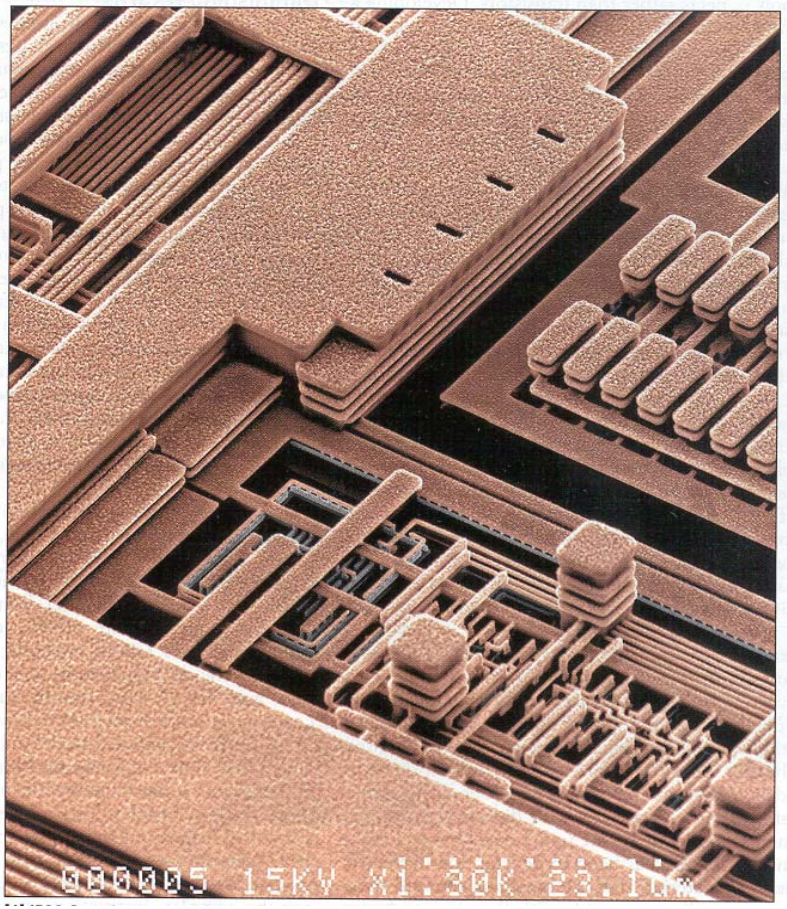
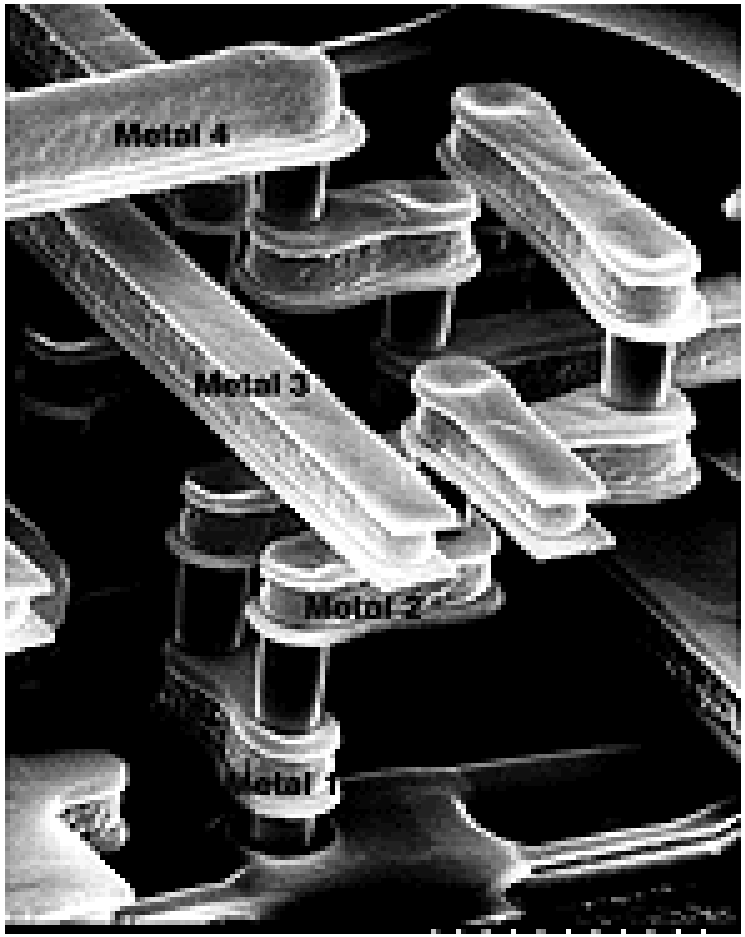
Advanced Metallization



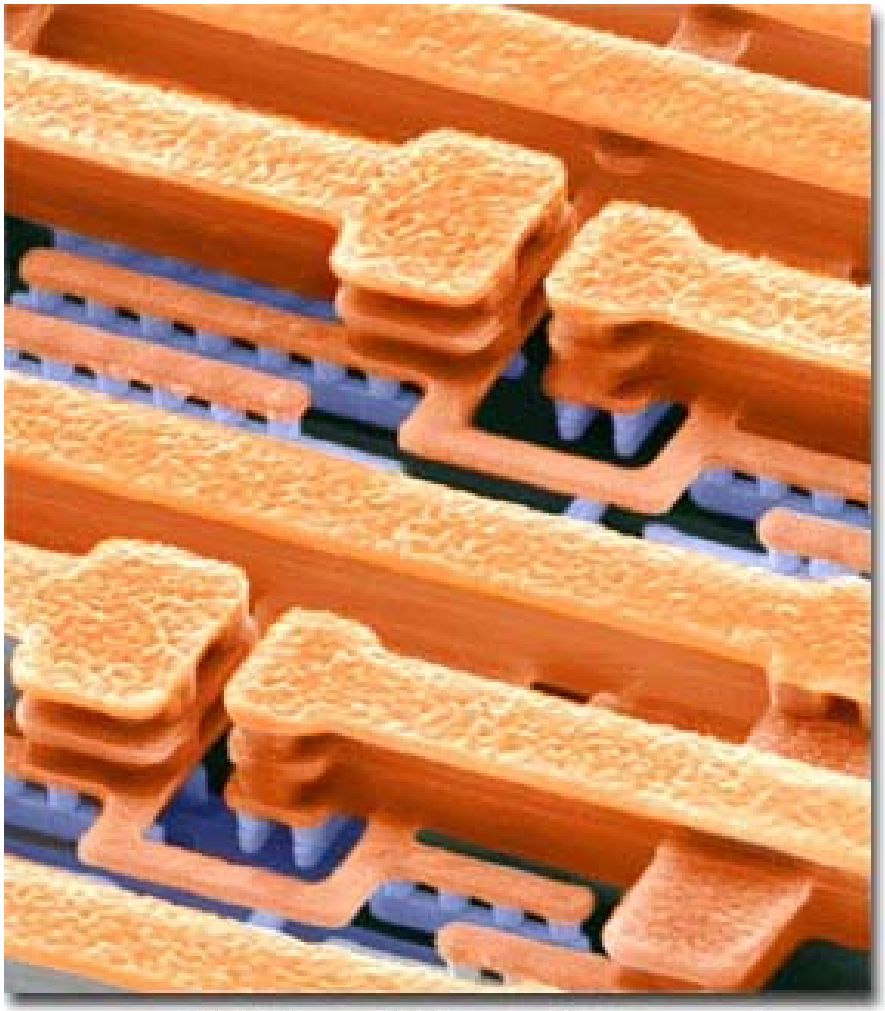


Courtesy, IBM

Advanced Matallization



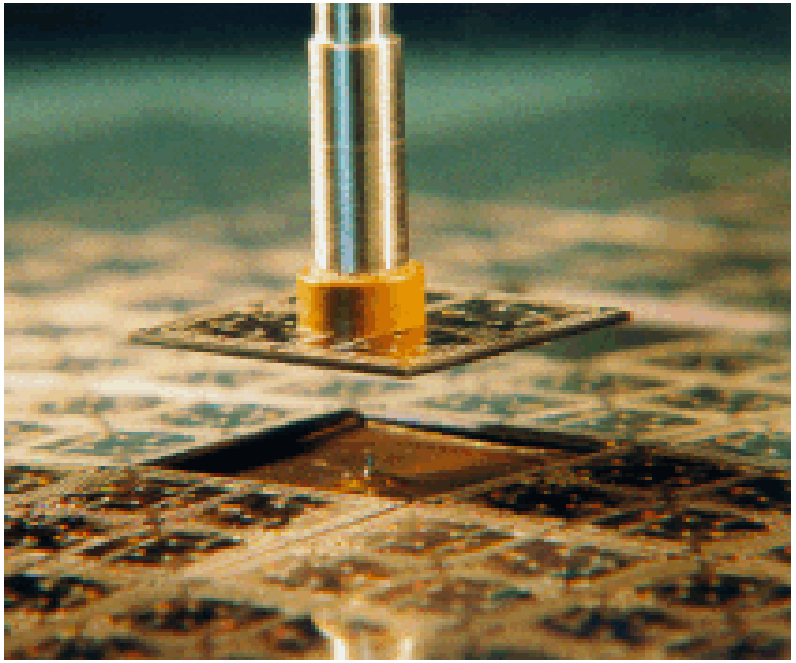
Advanced Metallization



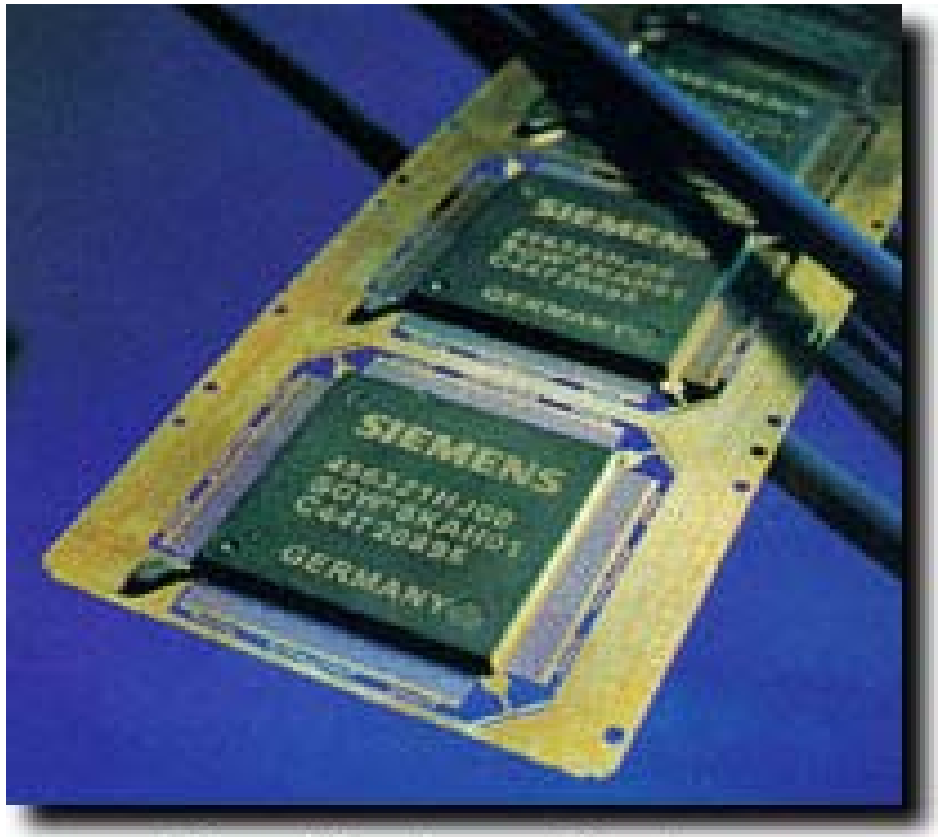
SEM view of Copper Interconnect
(IBM Microelectronics)

Courtesy, IBM

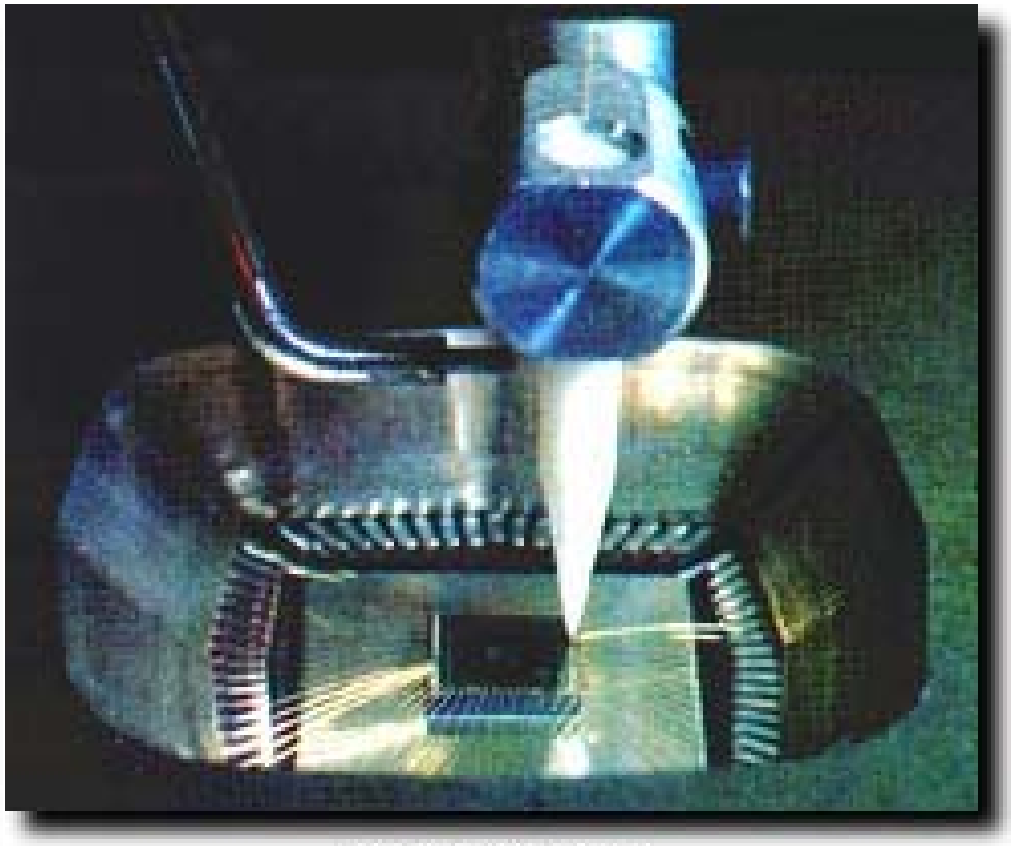
Packaging



Packaging

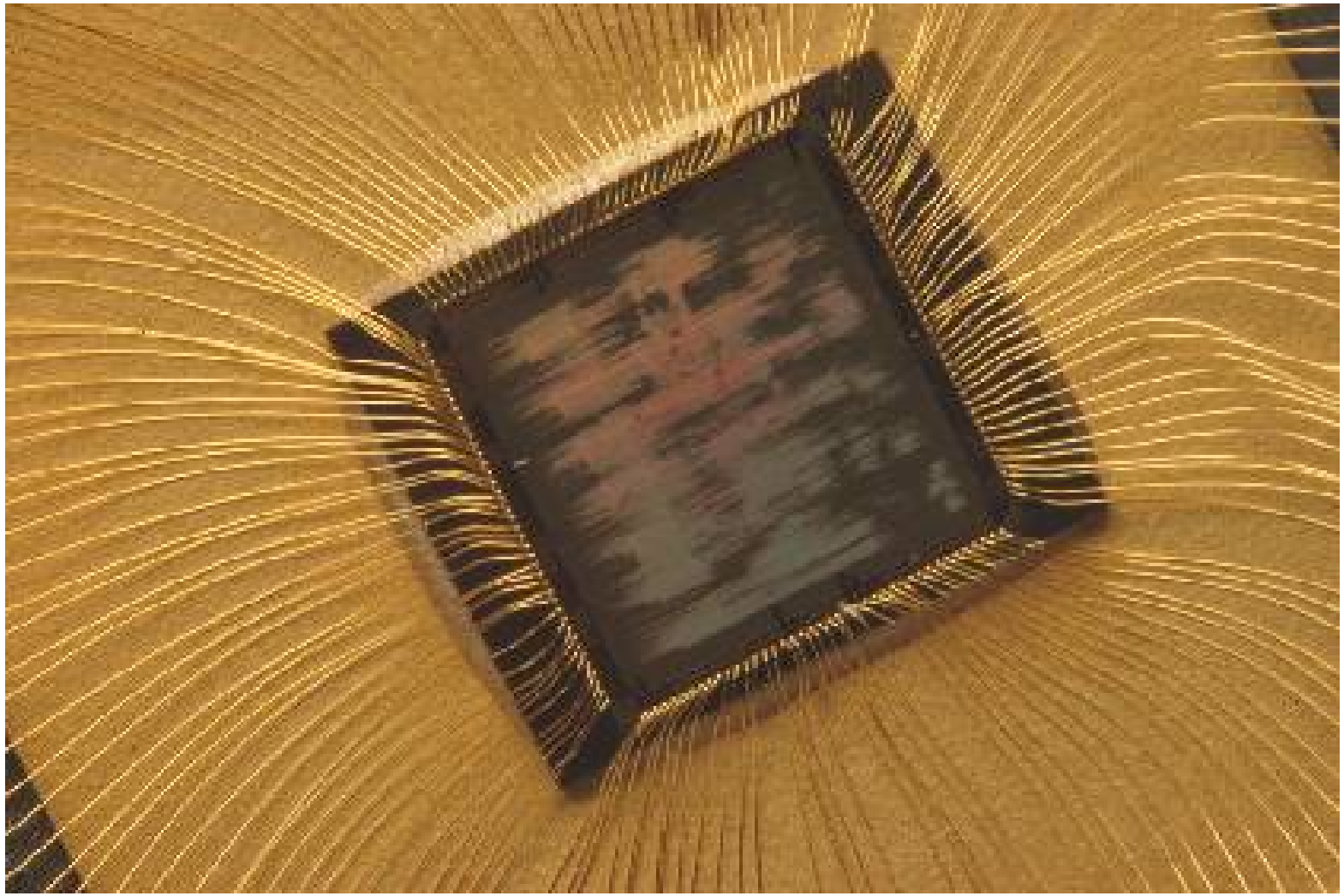


Quad Package Device
(Siemens AmG)



Wire Bonding
(Kulicke & Soffa Industries, Inc.)

Packaging



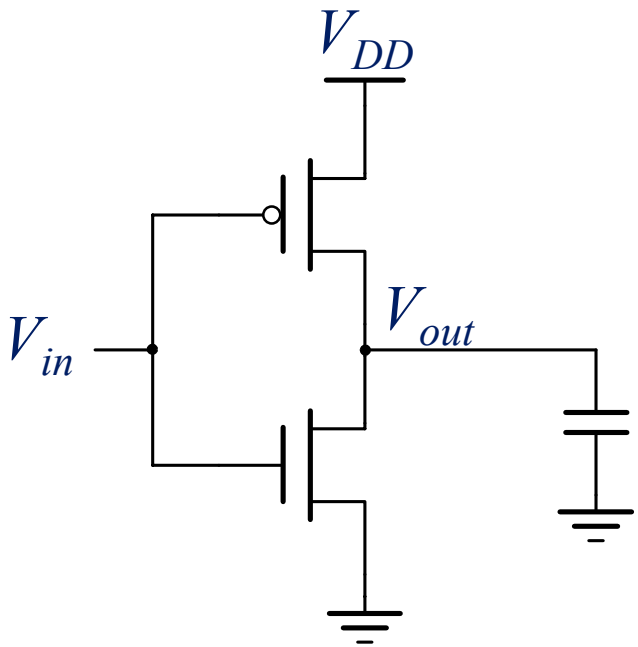
Outline

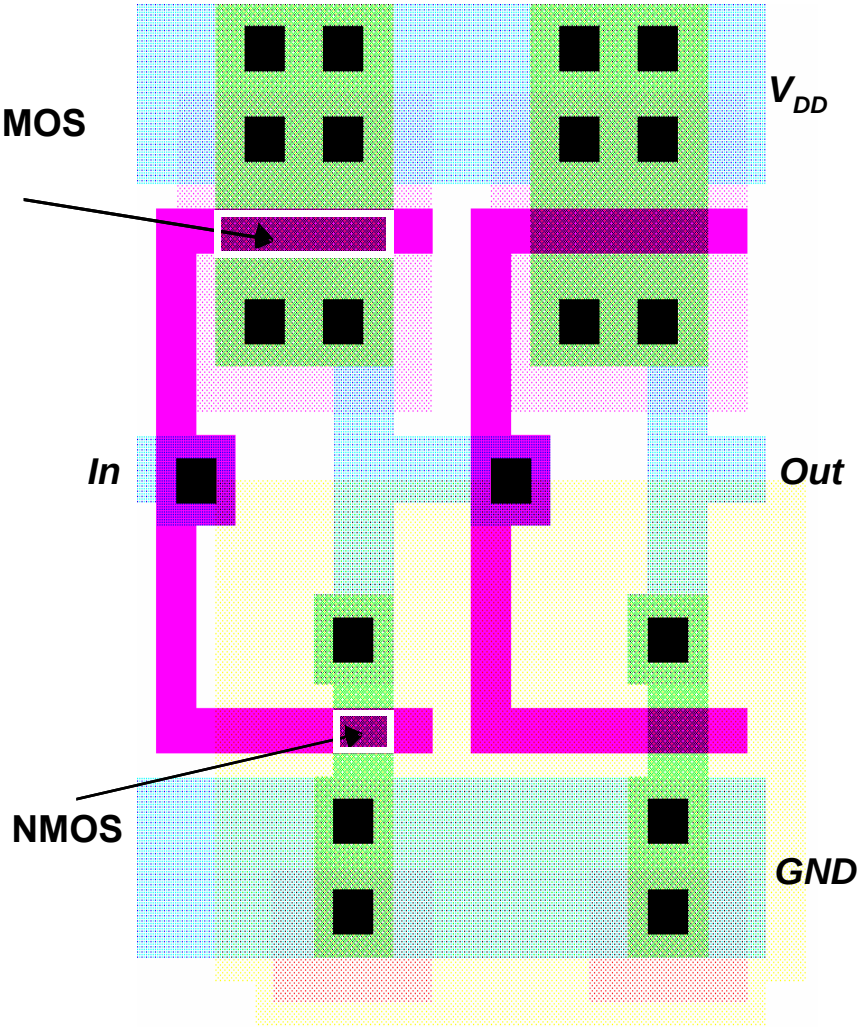
- Evolution from micro- to nano-electronics
- The ITRS and its impact on the research area
- Generalized device scaling
- Evolution of interconnects and packaging
- **Functional requirements of CMOS logic gates**
- New device architectures
- Device modeling issues
- Conclusions

Requirements of CMOS Logic Gates

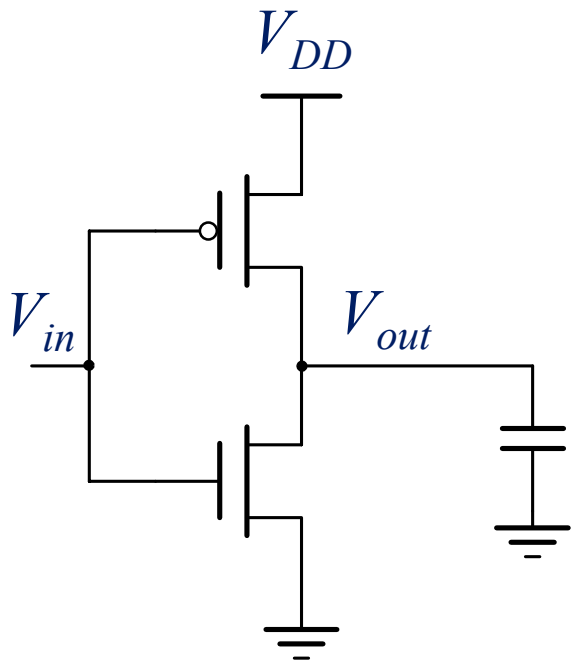
- High noise immunity → voltage gain
- High fan out → power gain
- High fan in → I/O isolation
- Compatibility of the I/O logic levels
- High switching speed
- Low power consumption

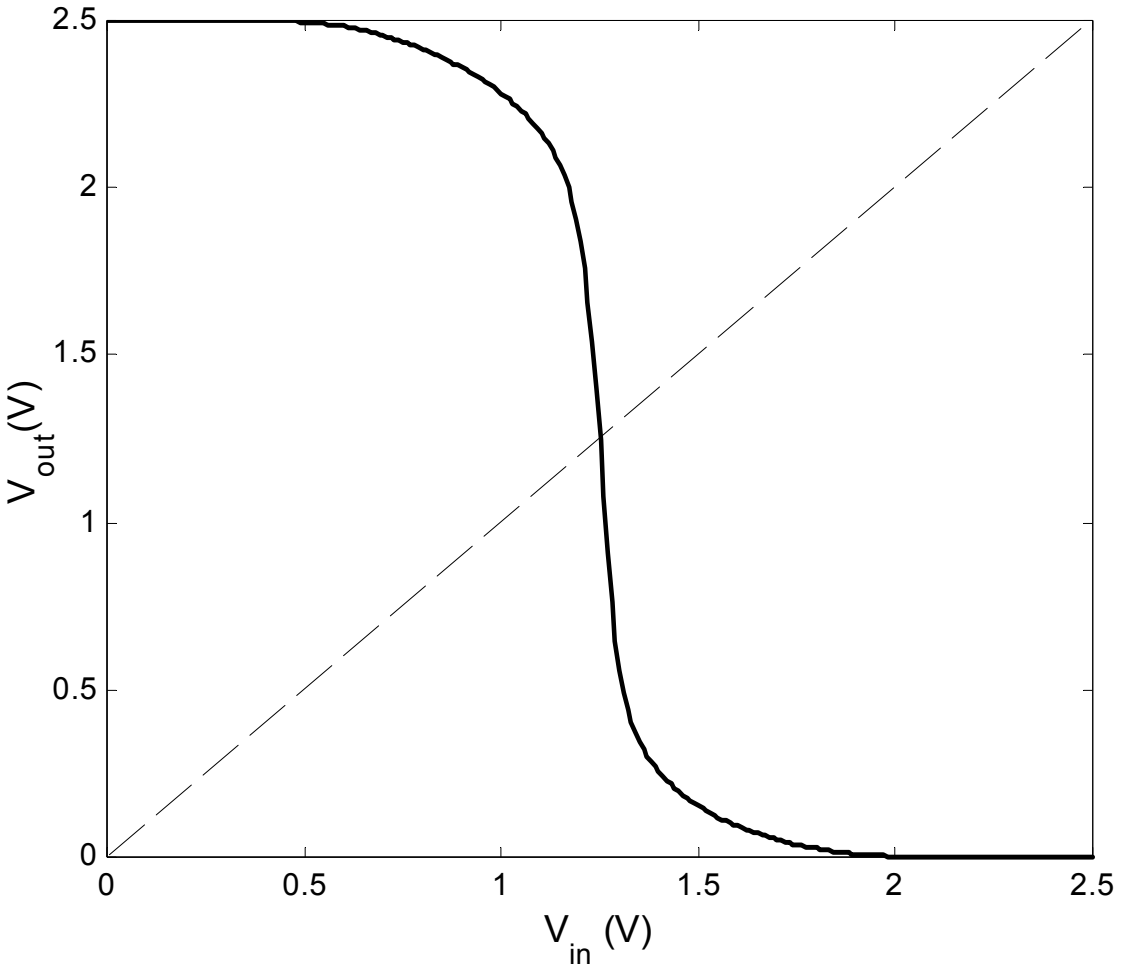
CMOS Inverter I/O Characteristics



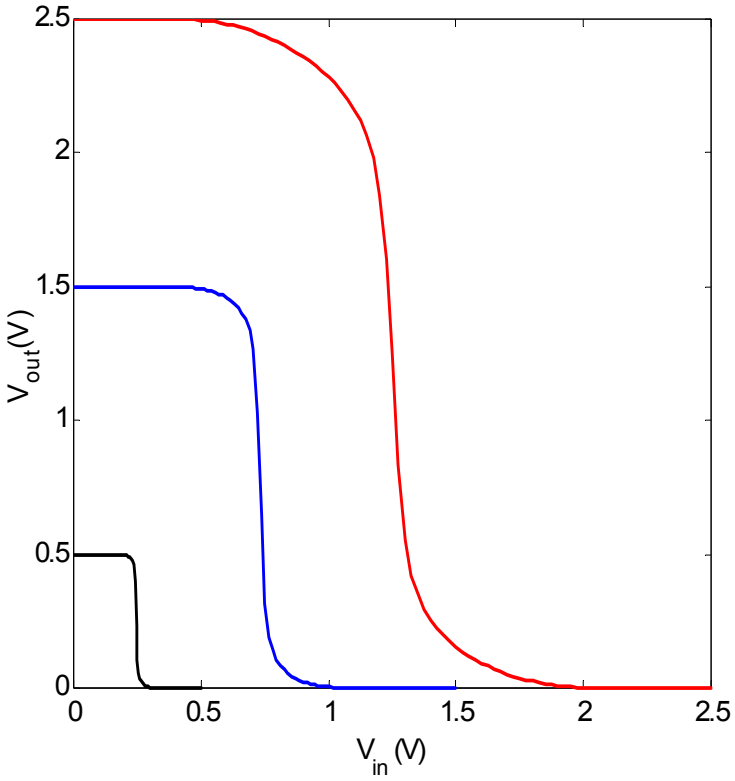


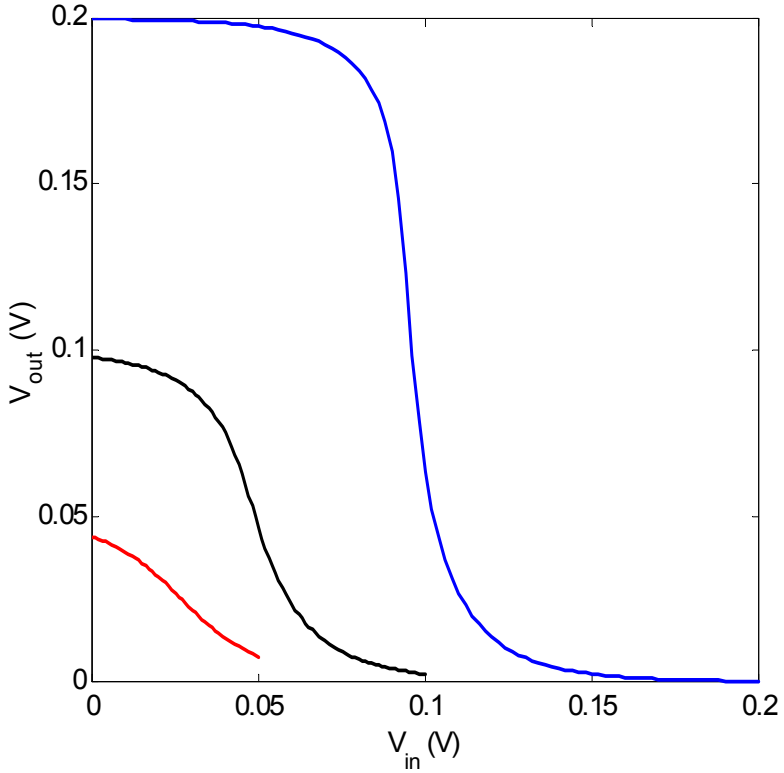
CMOS Inverter I/O Characteristics



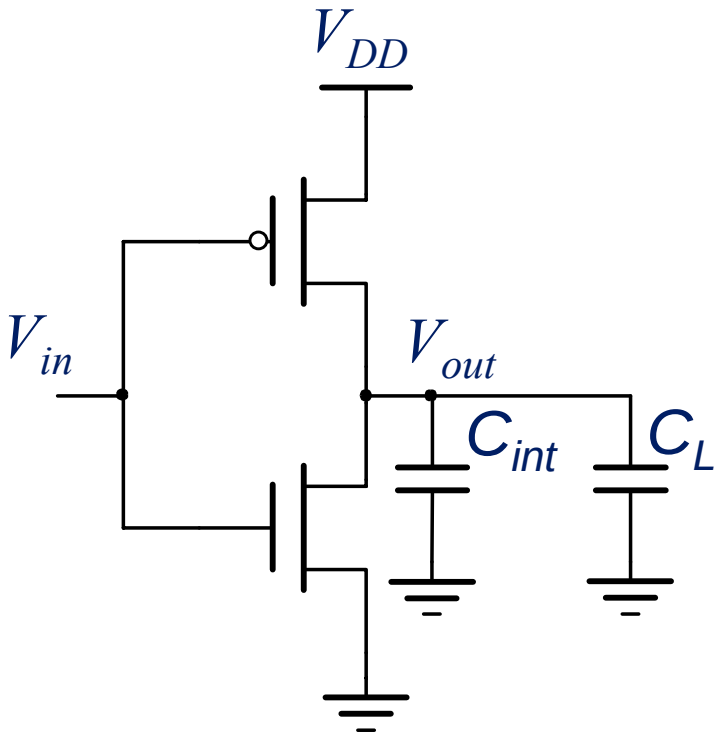


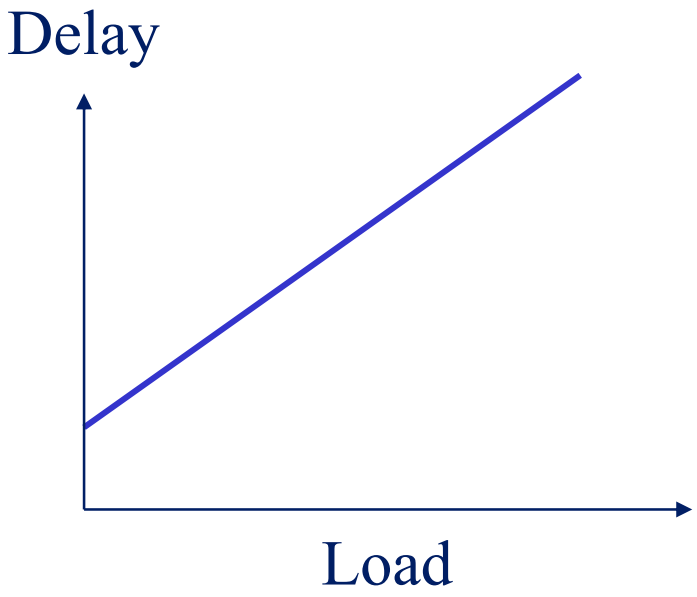
Gain vs. Supply Voltage





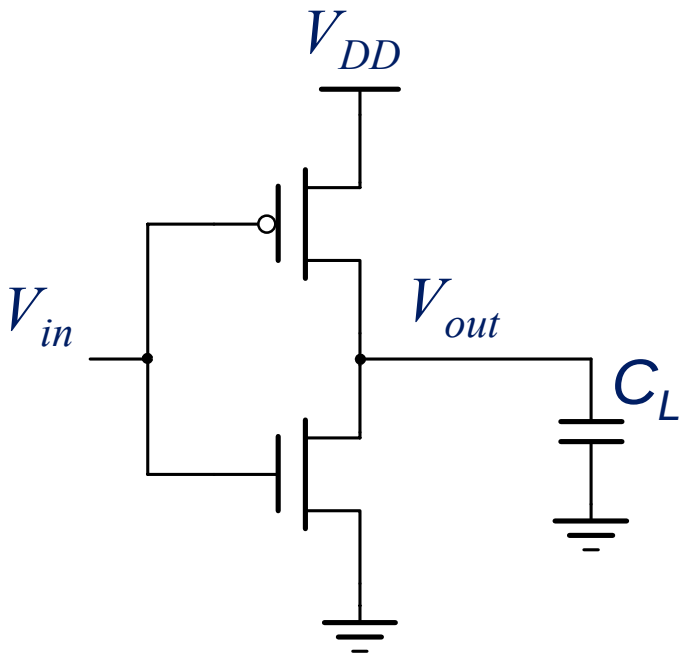
CMOS Inverter Delay





$$T_d \approx \frac{(C_L + C_{int})\, V_{DD}}{I_{DON}}$$

Energy Dissipation per Switch



$$E_d \approx C_L V_{DD}^2$$

Outline

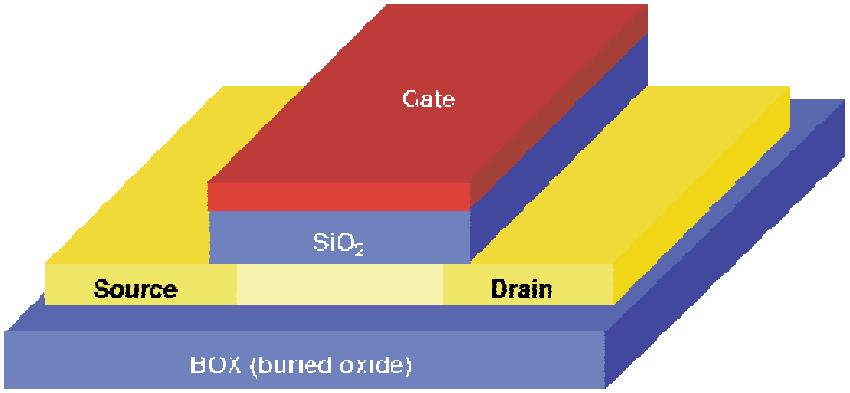
- Evolution from micro- to nano-electronics
- Device miniaturization and scaling theory
- The ITRS and its impact on the research area
- Evolution of interconnects and packaging
- Functional requirements of CMOS logic gates
- **New device architectures**
- Device modeling issues
- Conclusions

Alternative Device Architectures

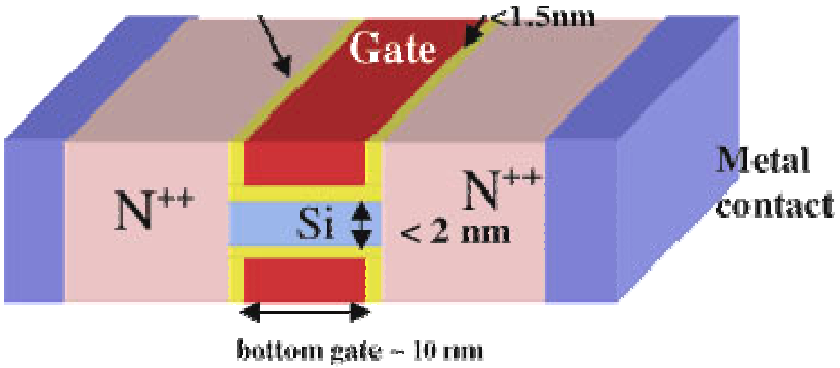
In view of a number of roadblocks which prevent standard CMOS scaling according to the ITRS provisions, new device architectures are being investigated in order to exploit the ultimate potential of the CMOS technology. Among them

- Ultra-thin body silicon on insulator (UTB-SOI) FETs
  - Silicon on insulator double-gate (SOI-DG) FETs
- Tri-gate FinFETs
  - Gate all around silicon nanowire (GAA NW) FETs.

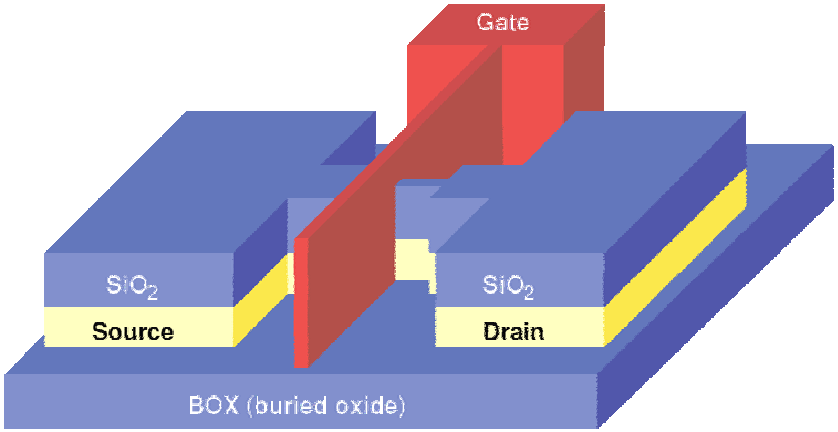
Alternative Device Architectures



SOI-MOSFET

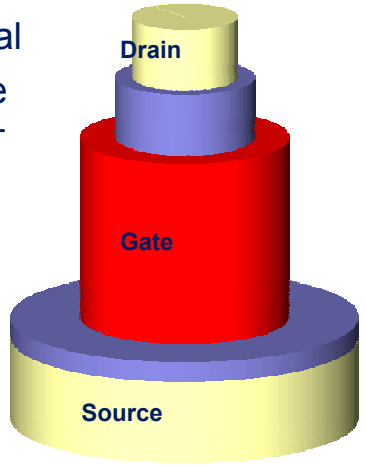


DG-MOSFET



FinFET

Cylindrical Nanowire MOSFET



CNW-FET

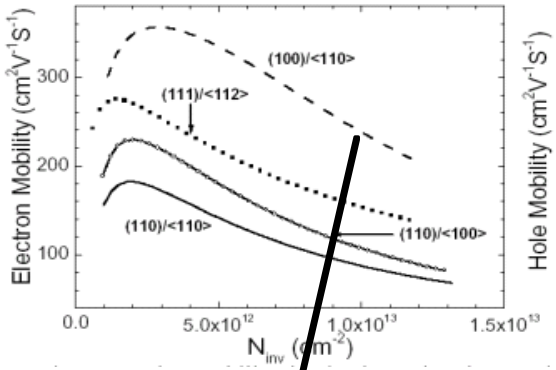
Bulk CMOS vs. New Architectures

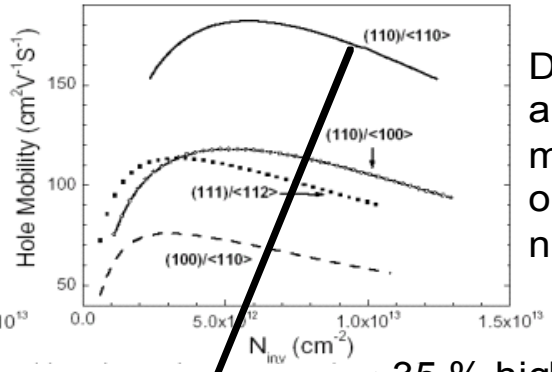
- The short-channel effect (SCE) is reduced as the gate control increases; thus, DIBL, SS and ΔV_t improve as we move from bulk to nanowire FETs for equivalent geometries
- For an acceptable DIBL, SS and ΔV_t , the electrical oxide thickness (EOT) scaling may be relaxed
- Undoped silicon channels prevent statistical doping fluctuation, improve mobility and reduce parasitic capacitance effects
- The presence of two or more channels improves the current drive capability of the FETs.

Bulk vs. New Architectures

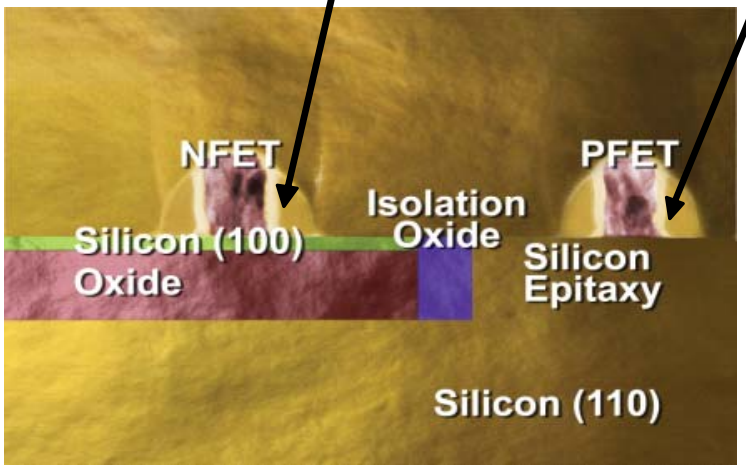
- In order to fully exploit the potential of innovative architectures technology enhancements are being investigated
- High-κ dielectrics for gate isolation, to increase the insulator capacitance while keeping a thicker oxide to prevent tunneling effects
- Metal gate to replace polycrystalline silicon gate, to prevent poly depletion at the poly-oxide interface
- Tensile and compressive stress to enhance channel mobility

Transport on (110) Surface

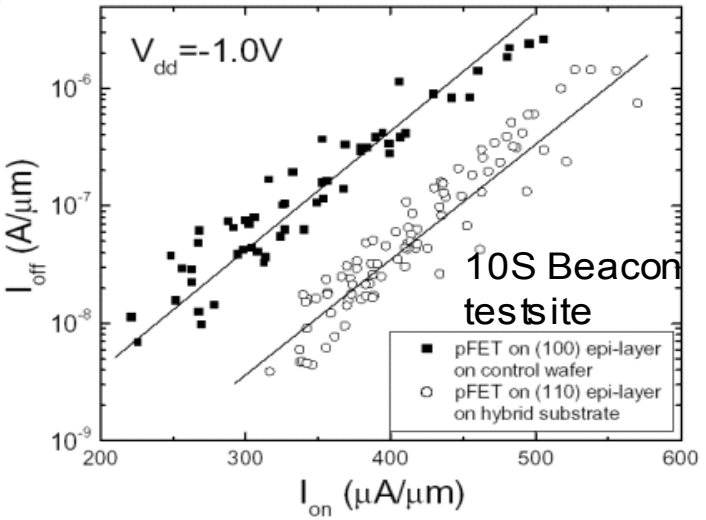




Developed substrate and processes of high mobility surface orientation for both nFETs & pFETs



~35 % higher pFET Idsat



10S Beacon testsite

Outline

- Evolution from micro- to nano-electronics
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- Conclusions

Electrostatics Solution

Classical solution:

$$-\nabla(\varepsilon\nabla(\varphi)) = q(p - n + N)$$

$$\begin{cases} n = n_i e^{\frac{q(\varphi-\varphi_F)}{KT}} \\ p = n_i e^{\frac{q(\varphi_F-\varphi)}{KT}} \end{cases}$$

➡ non linear differential equation.

QM solution:

$$-\nabla(\varepsilon\nabla(\varphi)) = q(p - n + N)$$

$$n = f_n[\psi(\varphi)]$$
$$p = f_p[\psi(\varphi)]$$

➡ ψ is the solution of the Schrödinger problem.

➡ A coupled Schrödinger-Poisson solution must be worked out.

Electrostatic Solution

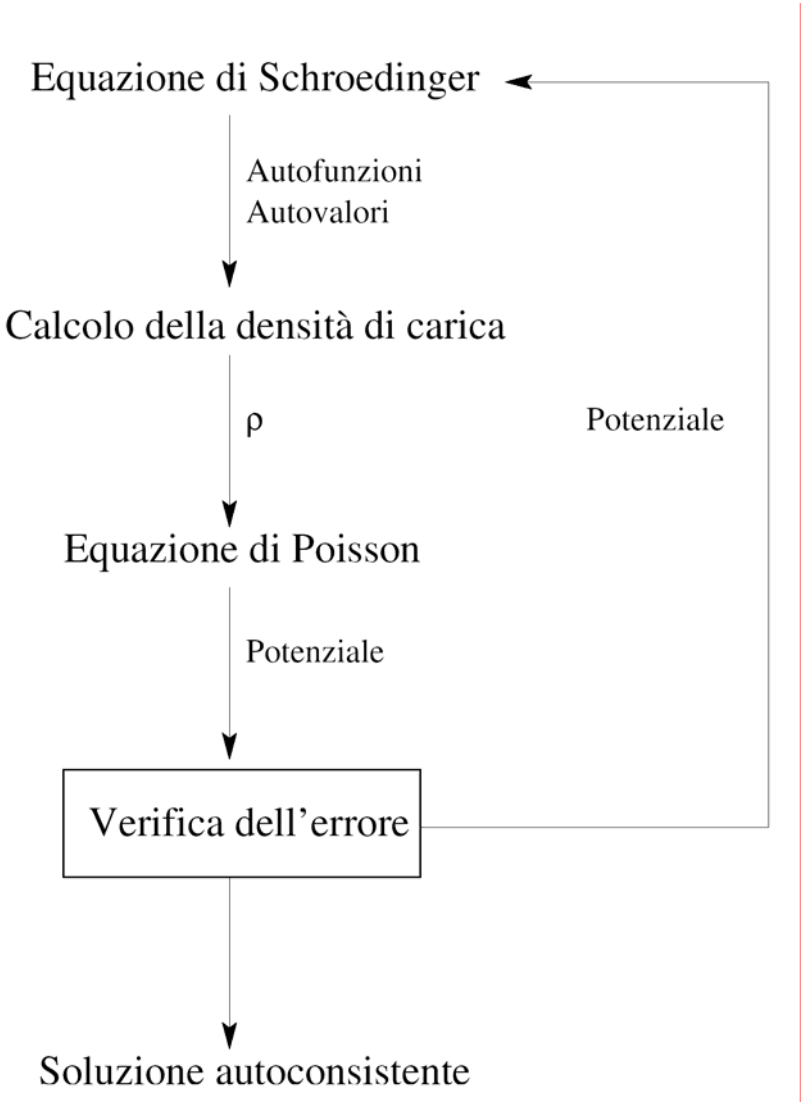
$$-\frac{\hbar^2}{2m^*}\frac{d^2\psi}{dx^2}+V\psi=E\psi$$

$$\varrho(\mathbf{r})=-q\sum_i^N|\psi_i(\mathbf{r})|^2\phi_{-1/2}\left(\frac{E_F-E_i}{k_BT}\right)\sqrt{\frac{m^*}{2\pi\hbar}}$$

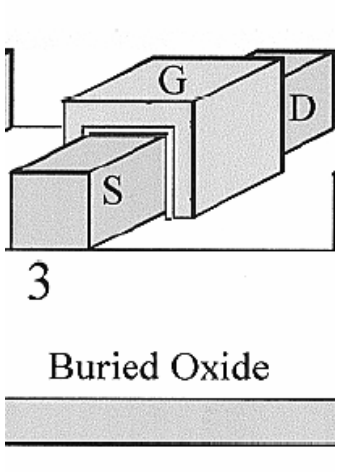
$$\nabla^2\delta\varphi+\frac{1}{\varepsilon}\left(\frac{\partial\varrho}{\partial\varphi}\right)\Big|_{\varphi=\varphi_0}\delta\varphi=-\frac{\varrho|_{\varphi=\varphi_0}}{\varepsilon}-\nabla^2\varphi_0.$$

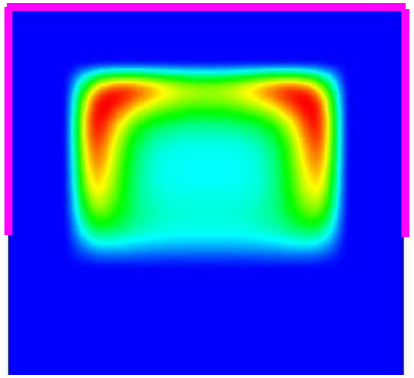
Potential φ

Charge density $\varrho(\mathbf{r})$

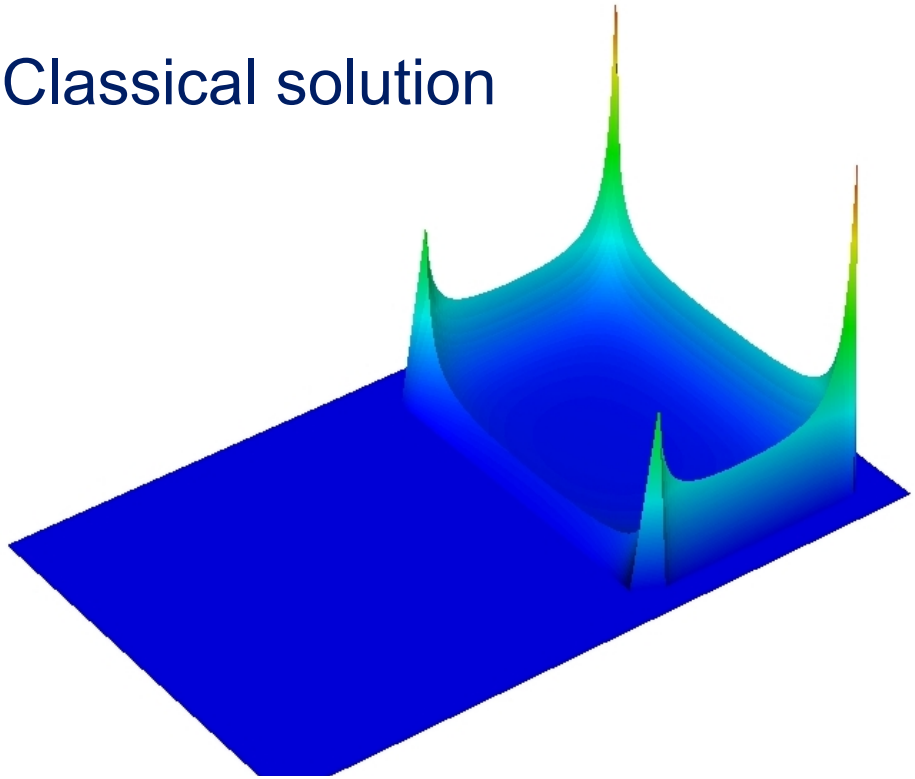


FinFET – Electron Density

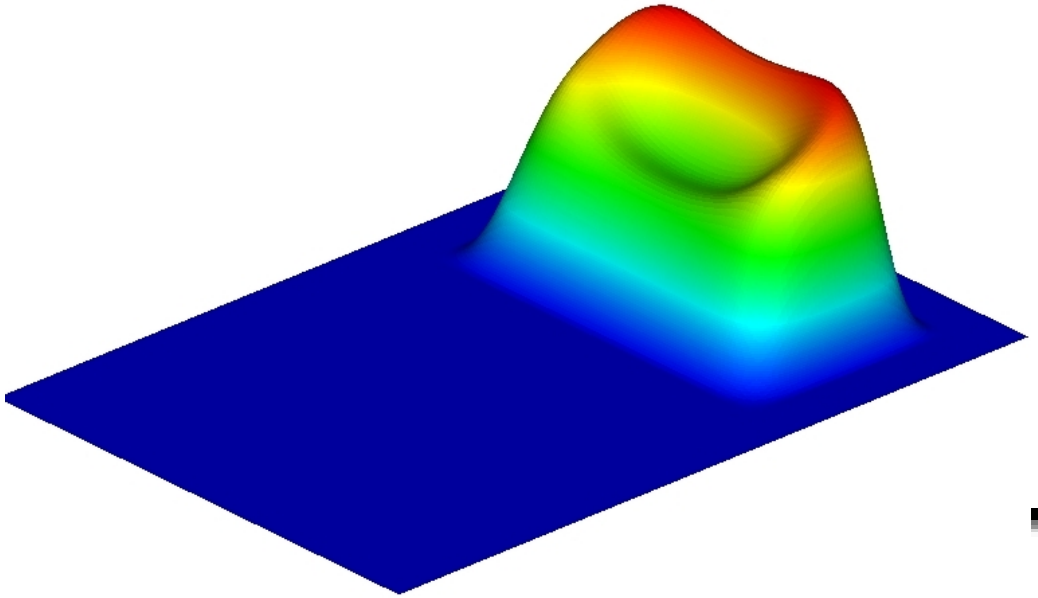




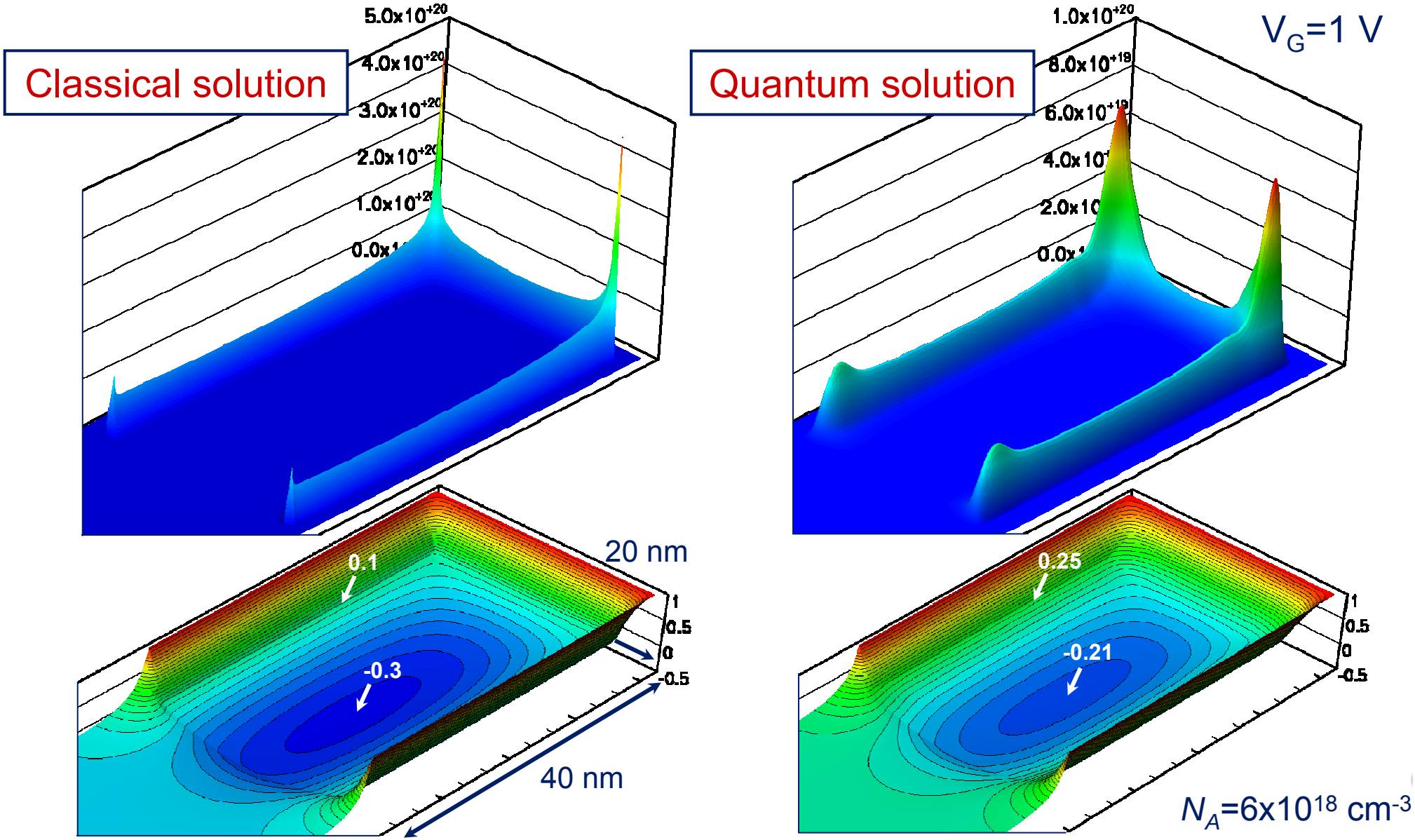
Classical solution



QM solution

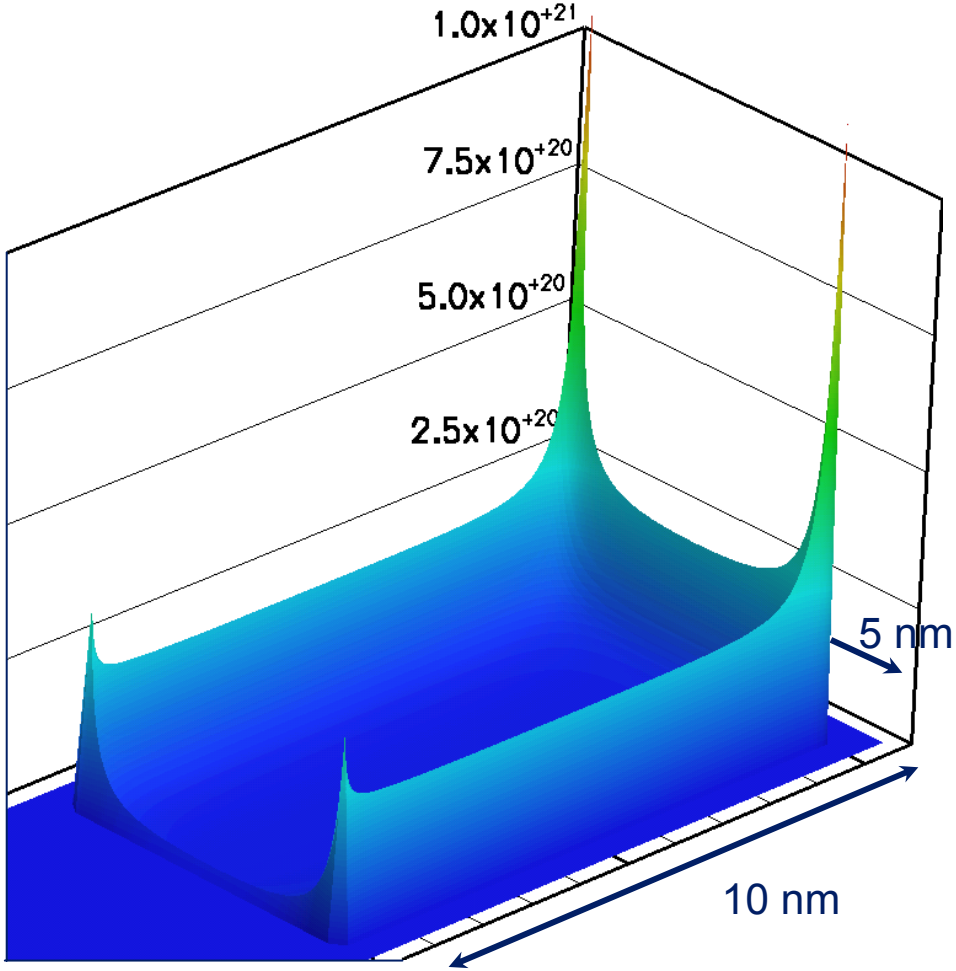


Electron concentration in the tri-gate FinFET (hp90)

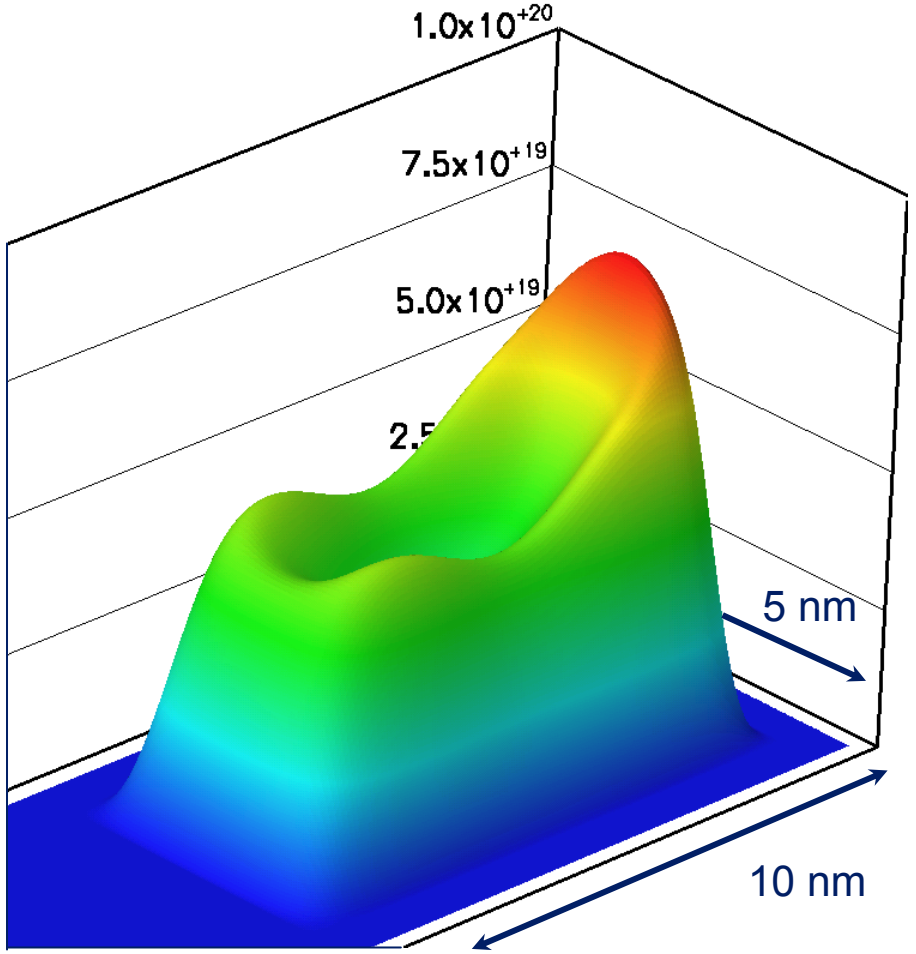


Electron concentration in the tri-gate FinFET (hp45)

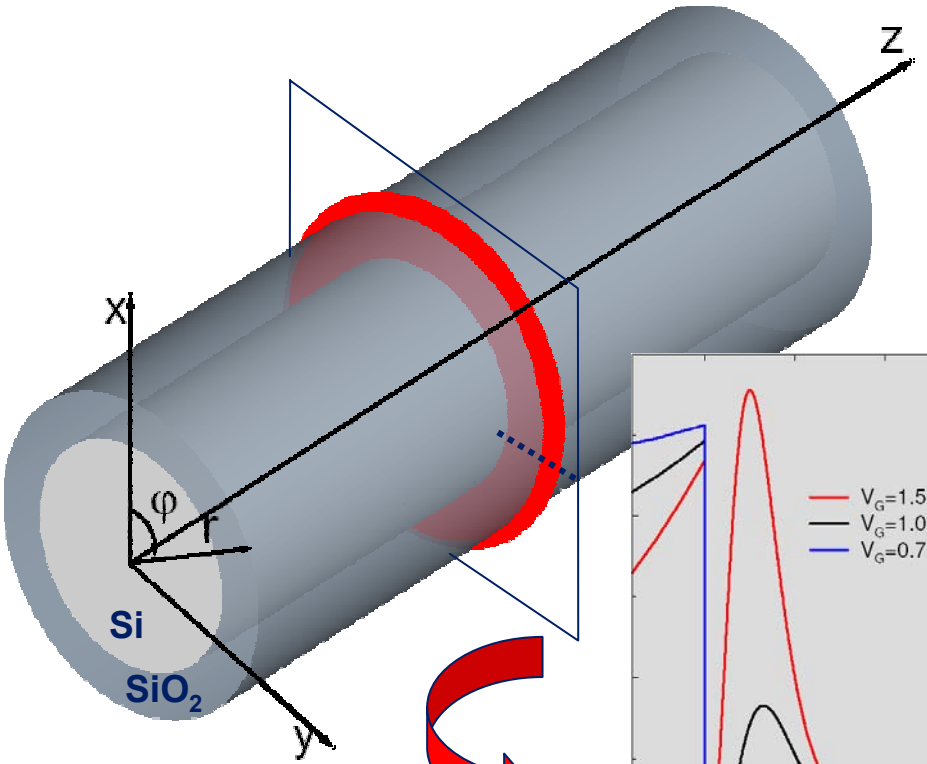
Classical solution

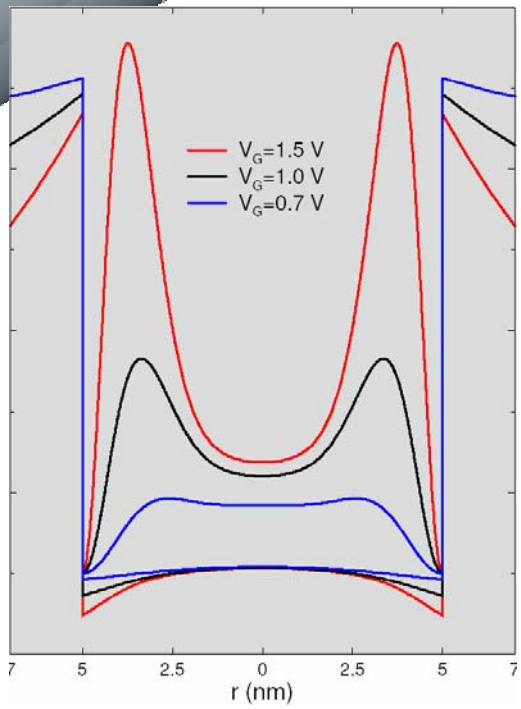


Quantum solution

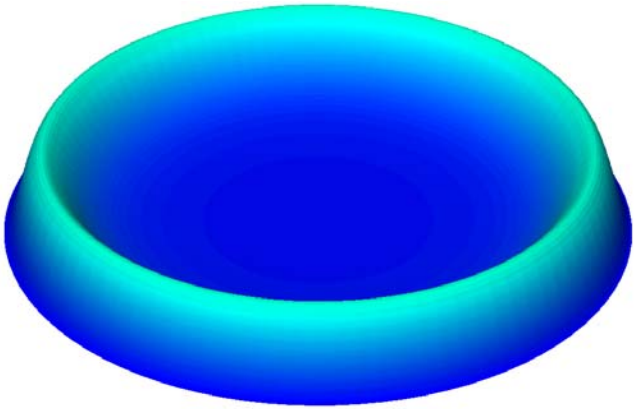


CNW-FET – Electron Density

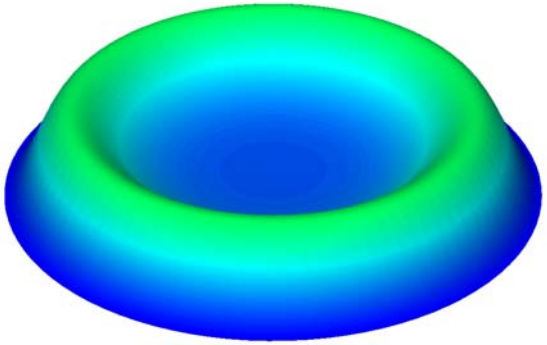




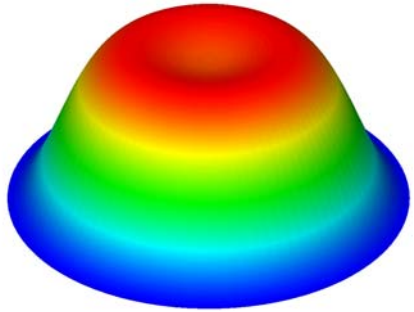
R=10nm



R=5nm

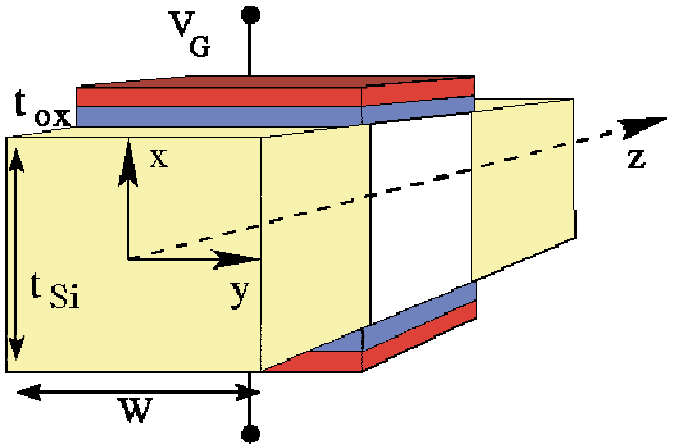


R=2.5nm

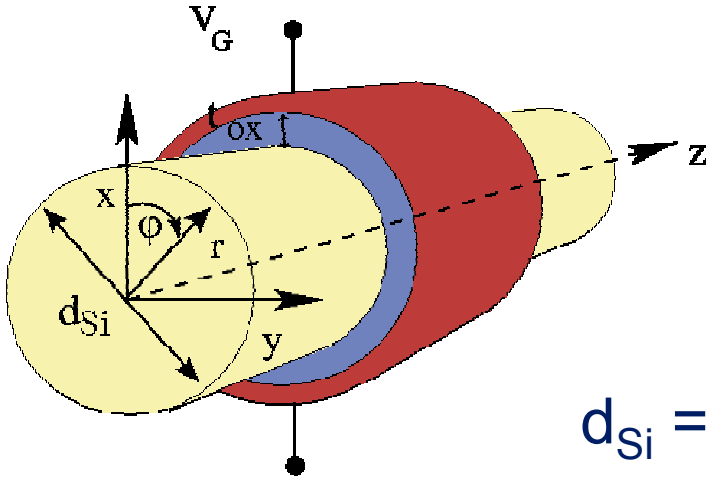


Current Transport in DG and CNW-FETs

Double-gate FET



Cylindrical nanowire FET



$d_{Si} = t_{Si}$

The DG-FET represents the best trade off between performance and manufacturability among the different multi-gate proposed structures.

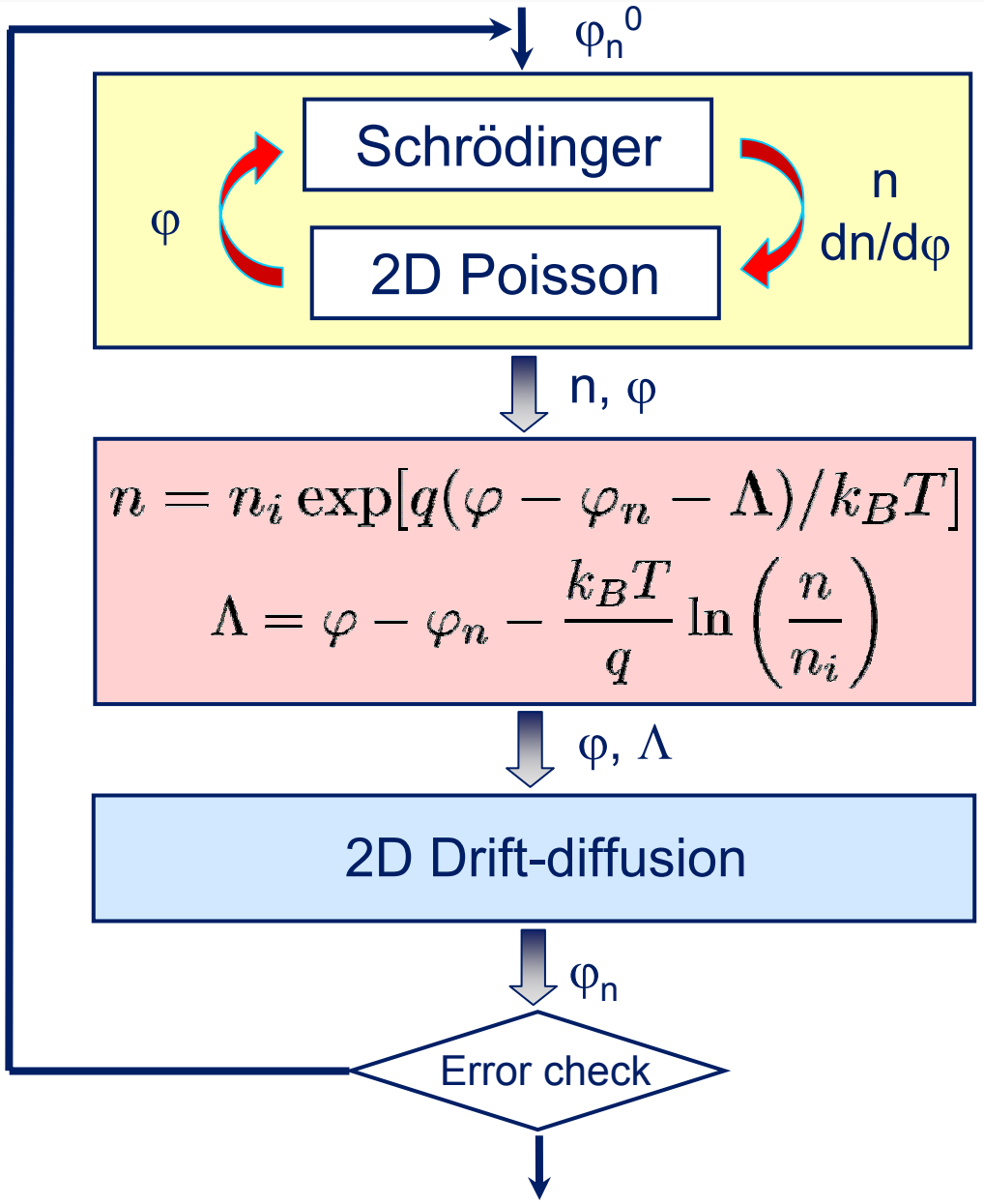
The CNW-FET is found to be one of the 1D silicon structures with the greater potential impact on scaled nanoelectronics.

Simulation Approach: Quantum DD

Solve the 2D coupled Schrödinger-Poisson problem

Extract the quantum potential from the Schrödinger-Poisson solution

Solve the 2D drift-diffusion equation to determine the quasi-Fermi potential



Simulation approach: full-quantum transport

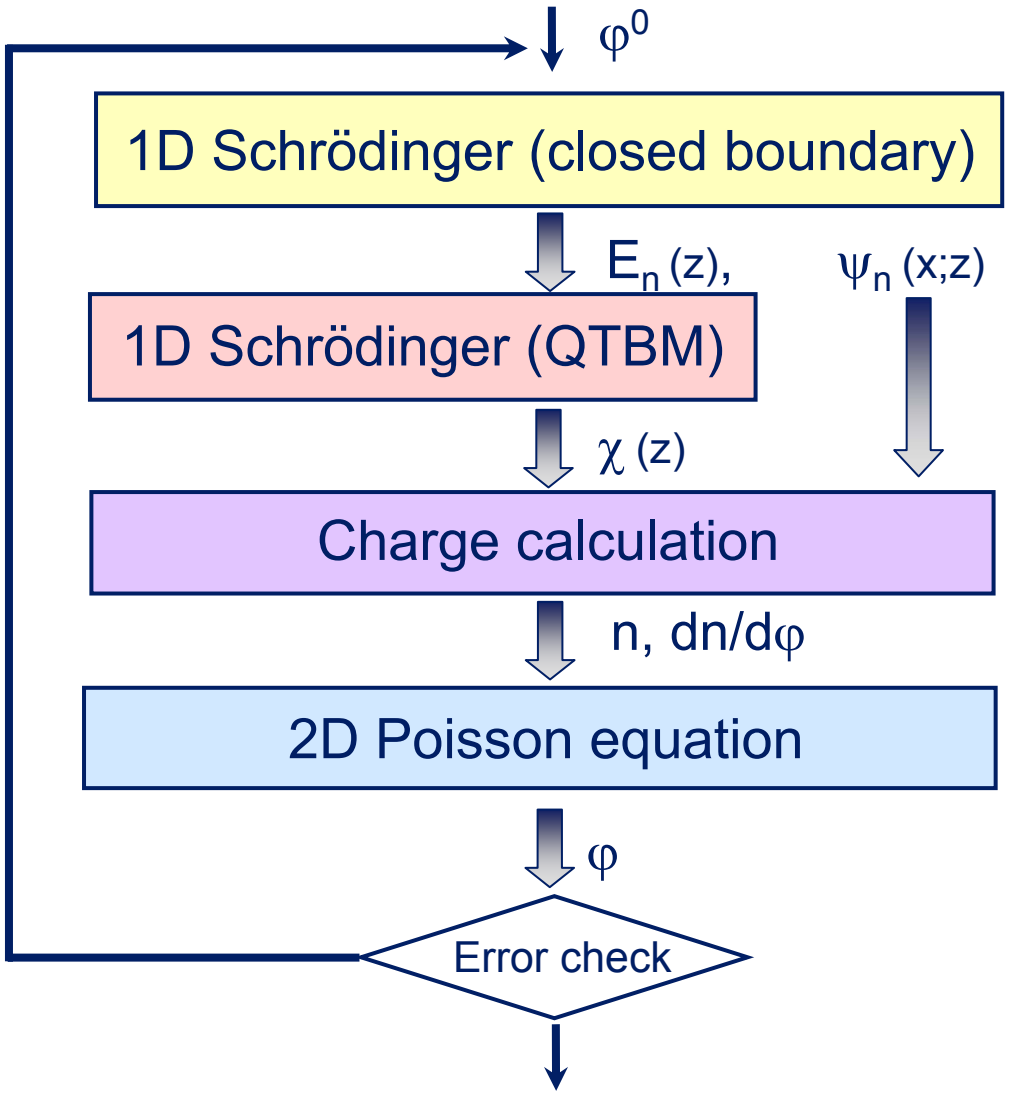
The problem is solved by decoupling the Schrödinger equation along the transverse and longitudinal coordinate:

Solve the 1D Schrödinger eq. normal to the interface for each node along the channel

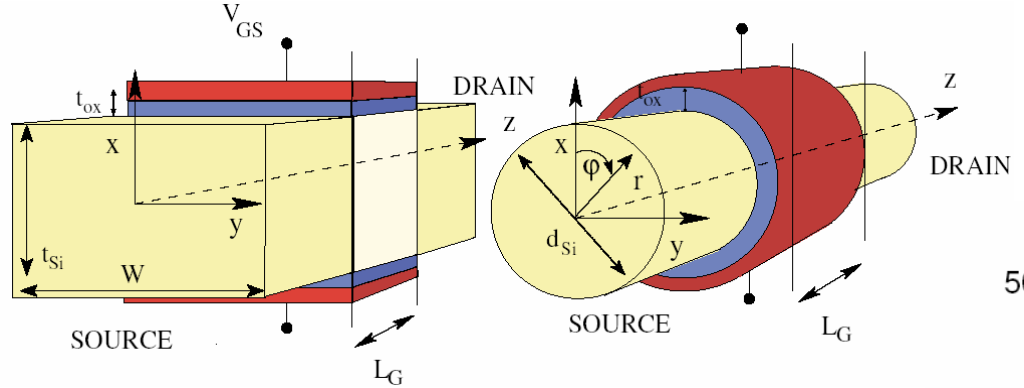
Solve the 1D Schrödinger equation with open boundary conditions

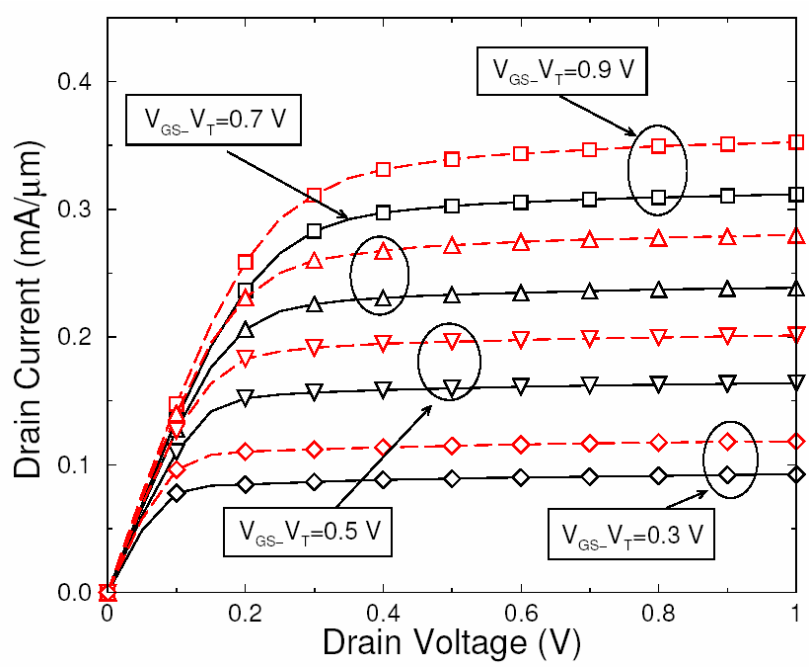
Calculate the charge density

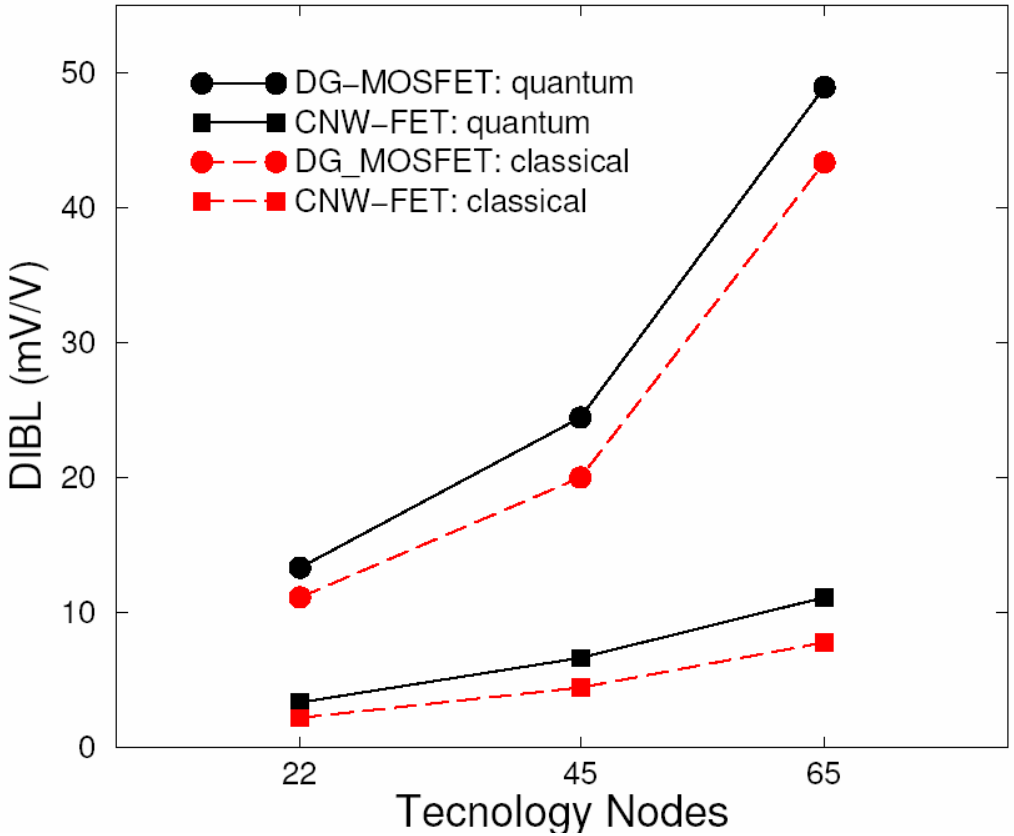
Solve the 2D Poisson equation



Comparison of device performance





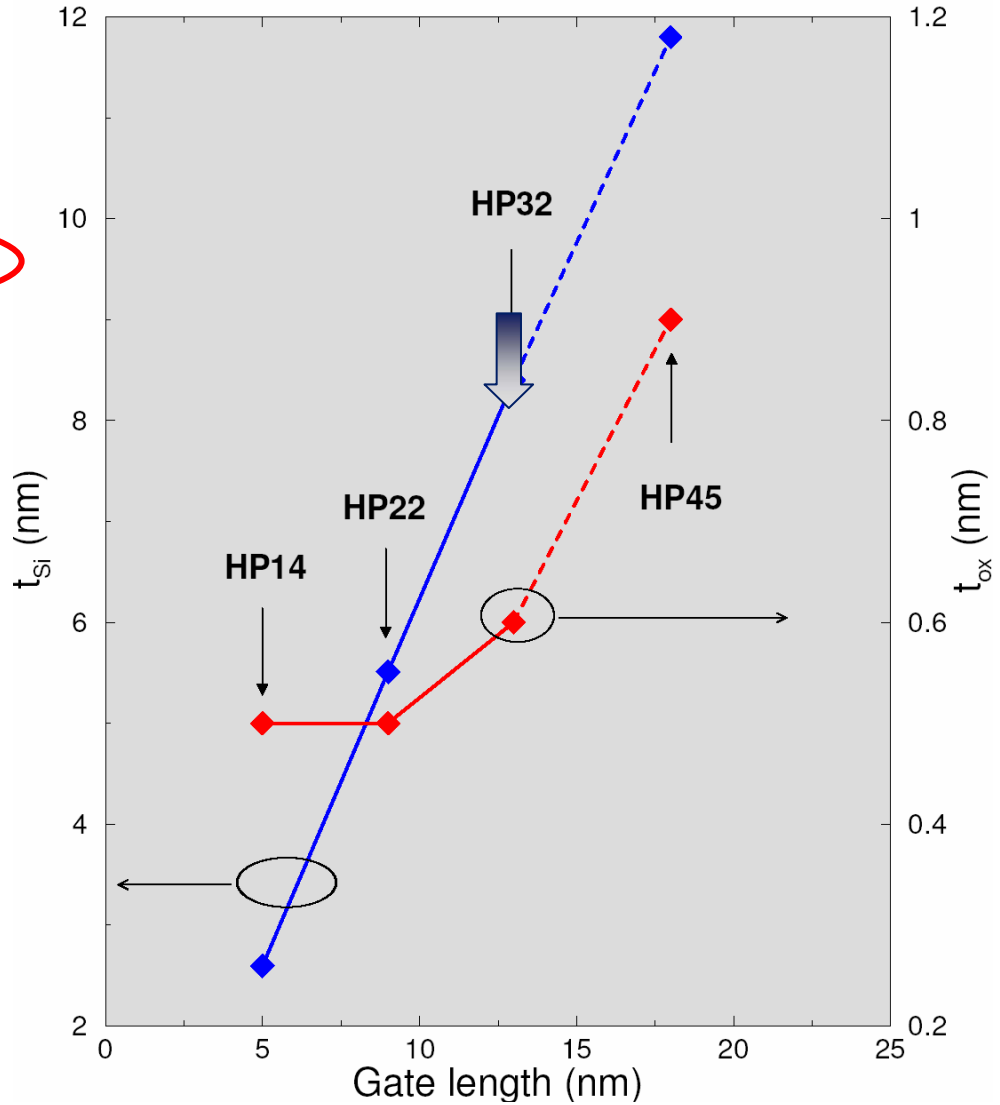


Scaling rules

	HP45	HP32	HP22	HP14
Year	2010	2013	2016	2020
Lg (nm)	18	13	9	5
EOT (nm)	0.9	0.6	0.5	0.5
t_{Si} (nm)	11.8	8.4	5.51	2.59
V_{DD} (V)	1.0	0.9	0.8	0.7
I_{off} (nA/um)	145	107	108	108

The electrical oxide thickness is expected to be scaled down to 0.5 nm for HP22 and HP14:

➡ gate leakage current



High-κ Dielectrics

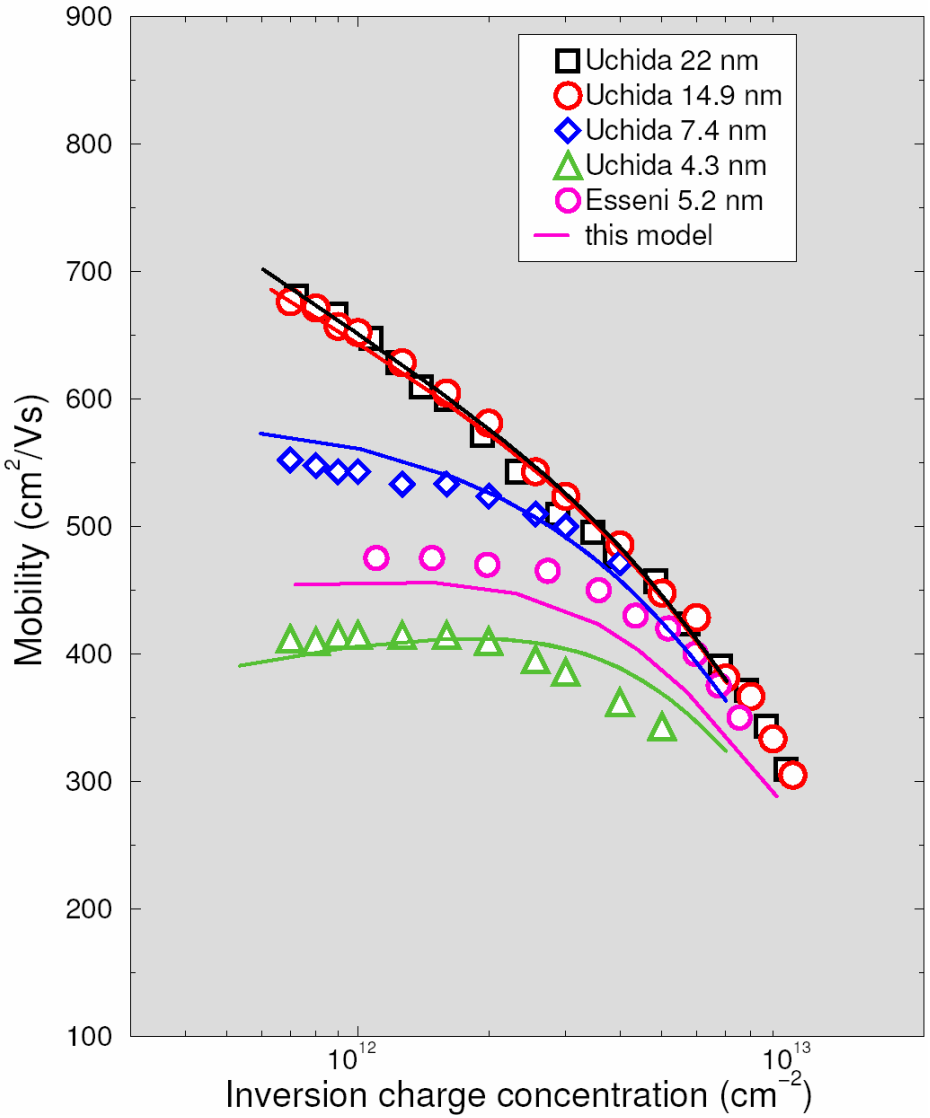
High-permittivity dielectrics are thoroughly being investigated as an alternative to the conventional silicon dioxide.

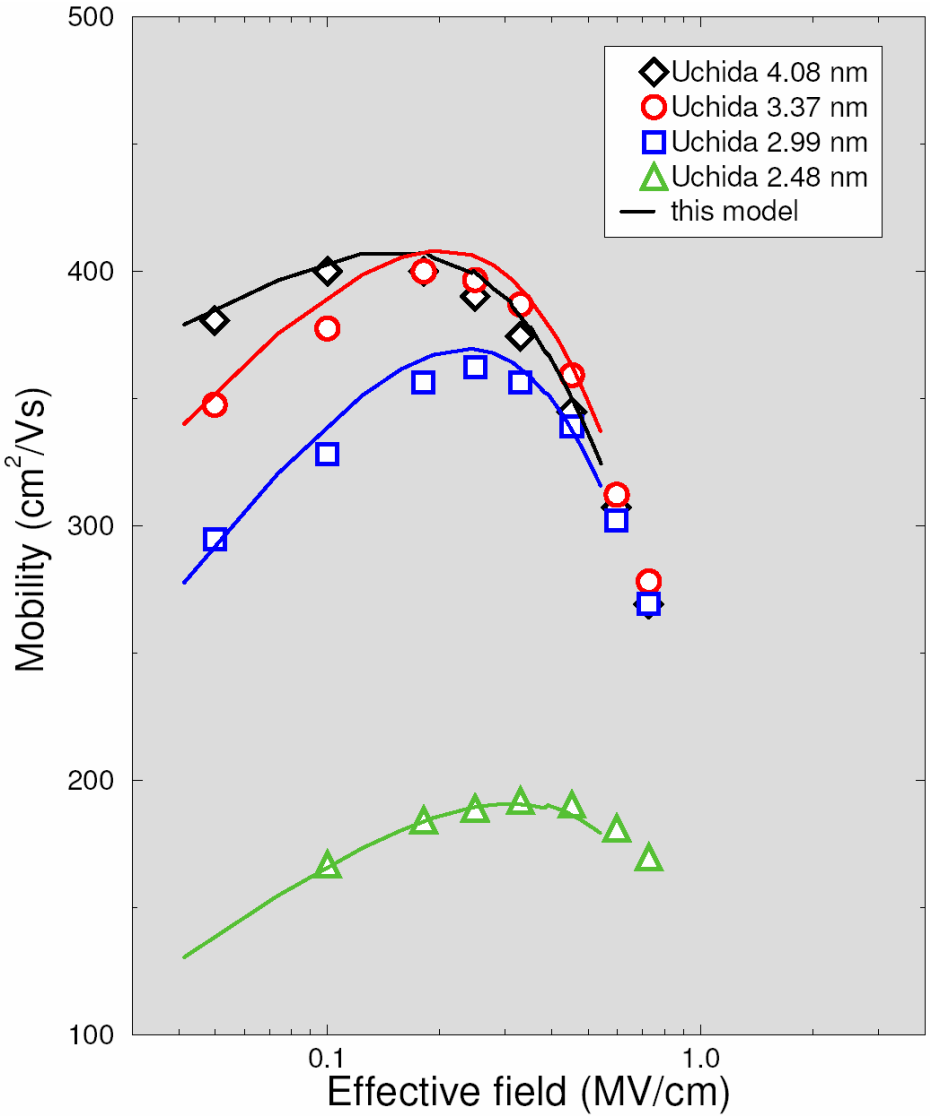
Hafnium oxide is one of the most promising candidates.

$$t_{HfO2} = \varepsilon_{HfO2} / \varepsilon_{SiO2}\ EOT \approx 6\ EOT$$

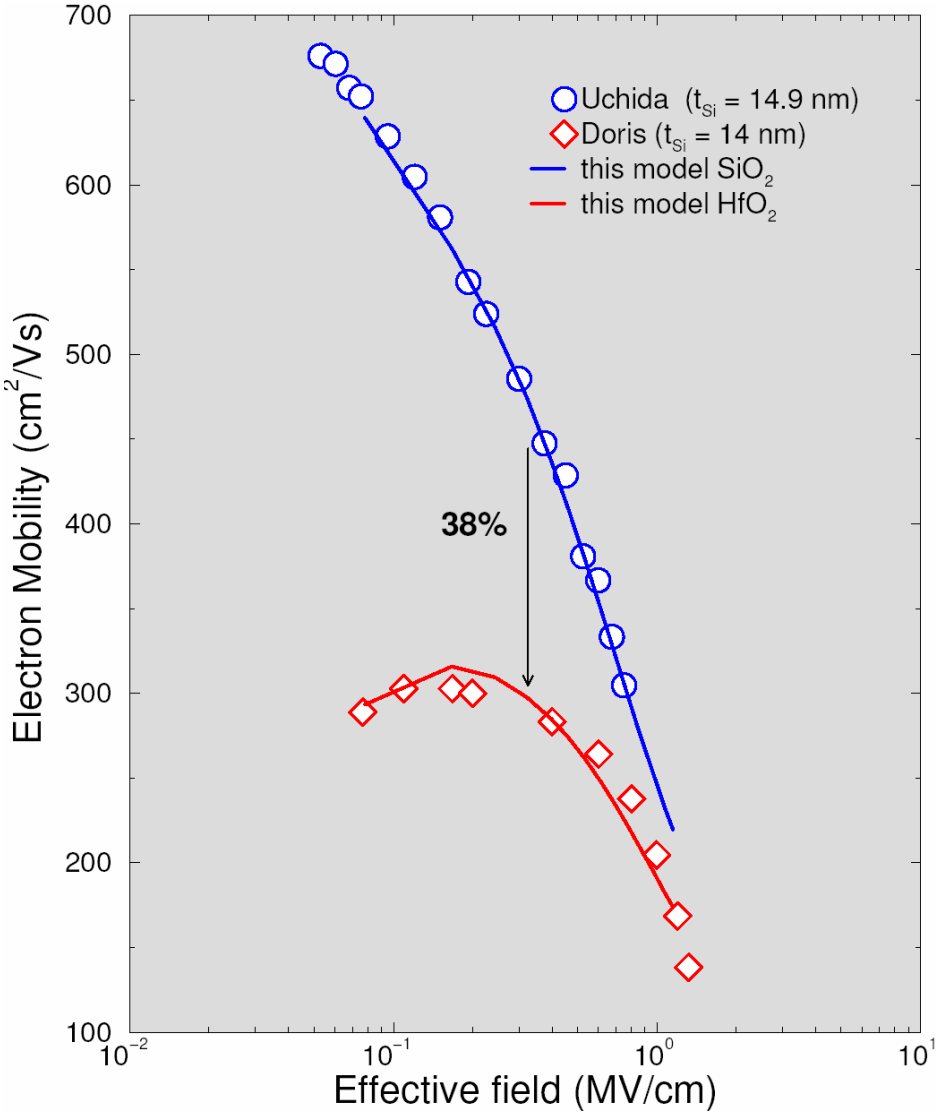
➡ A fundamental drawback of high-κ dielectrics is mobility degradation.

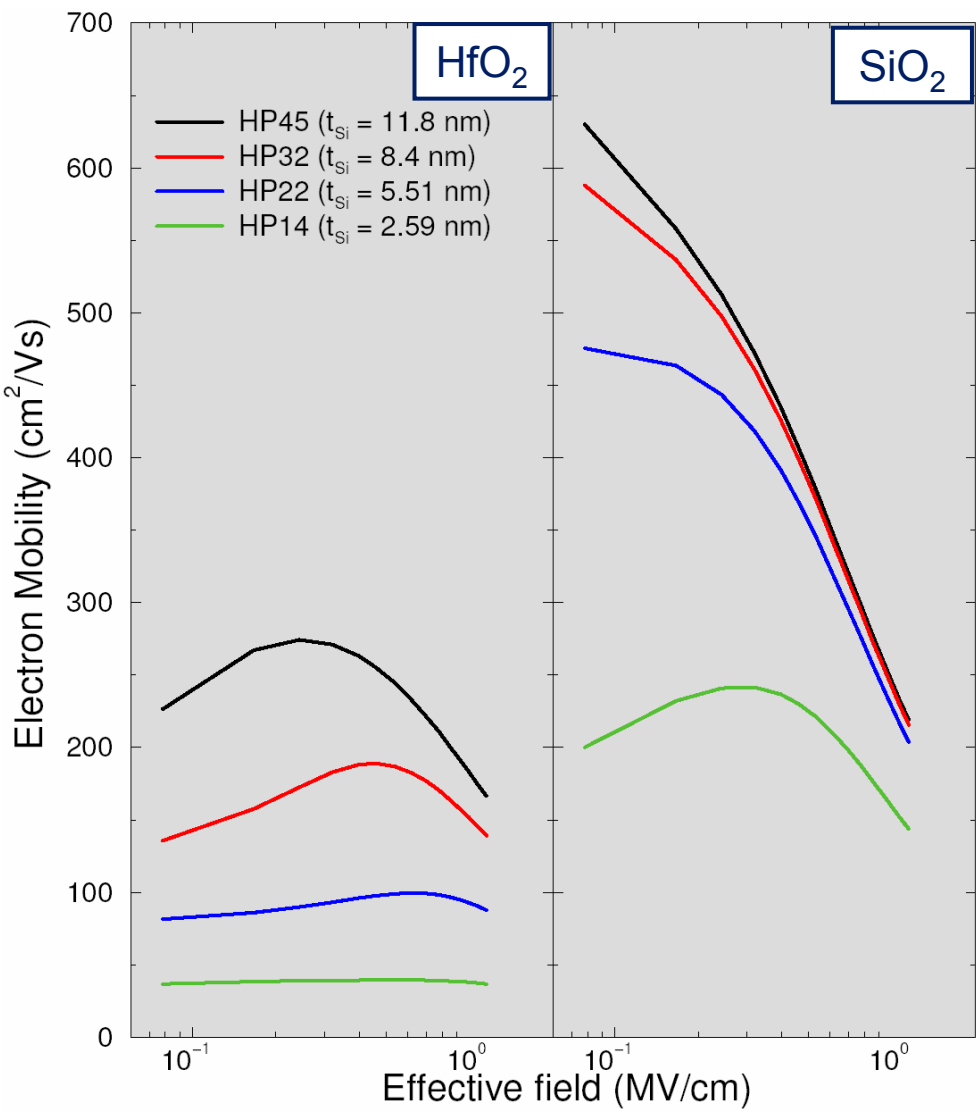
Mobility model



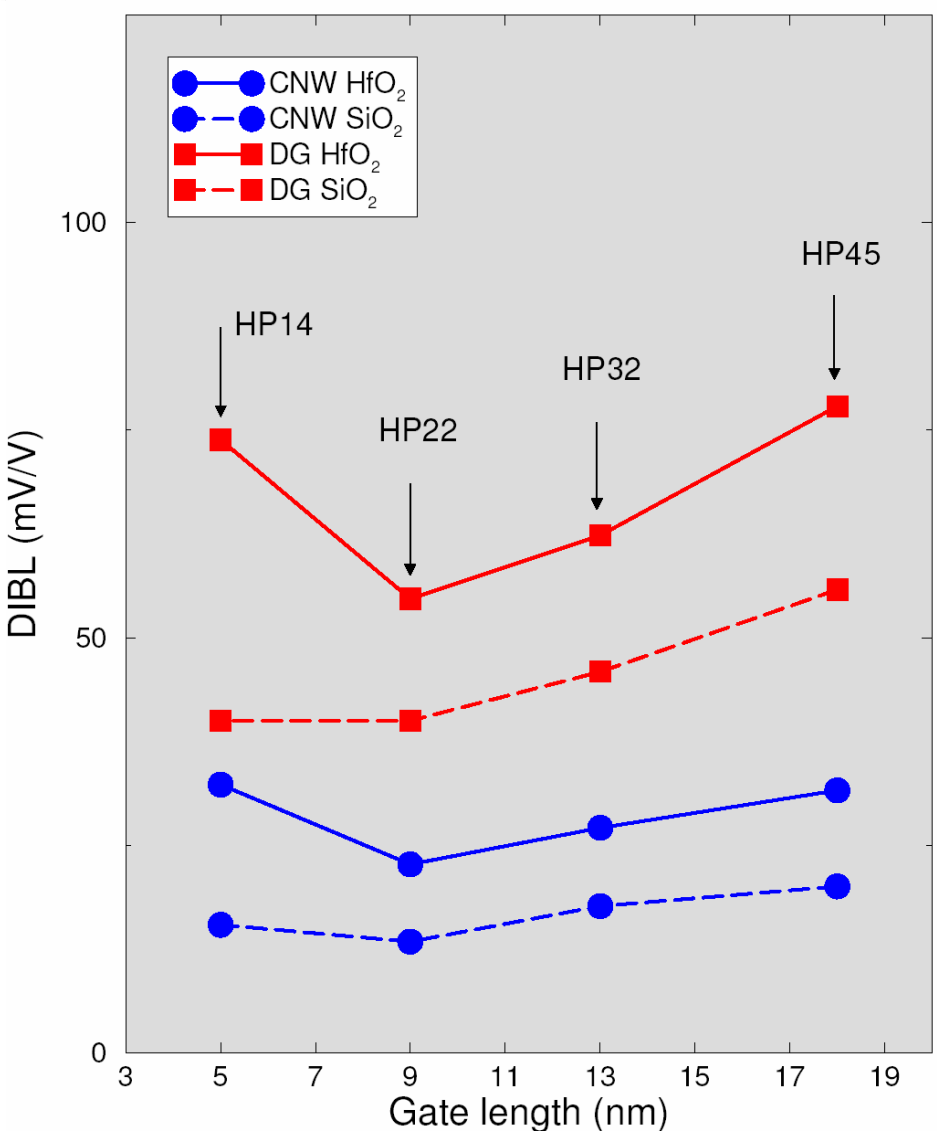


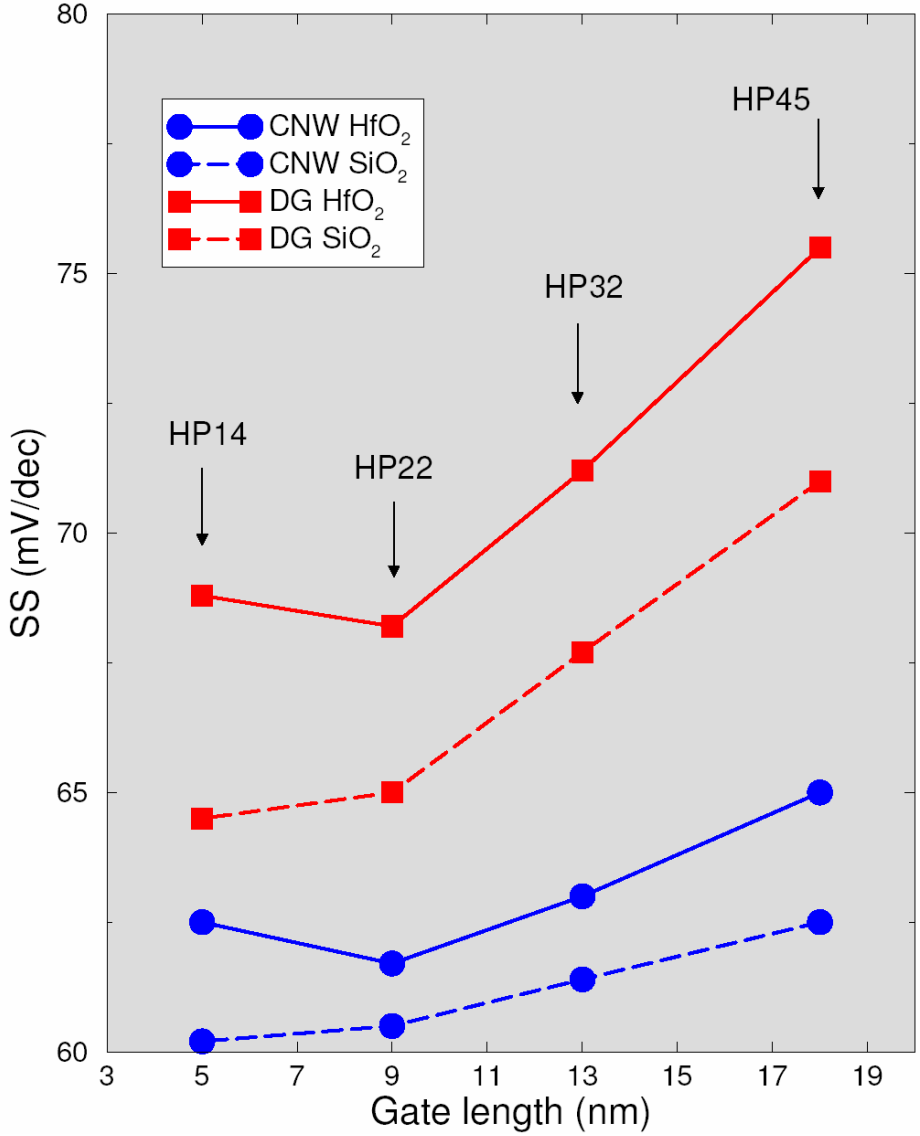
Mobility model for SiO_2 and HfO_2





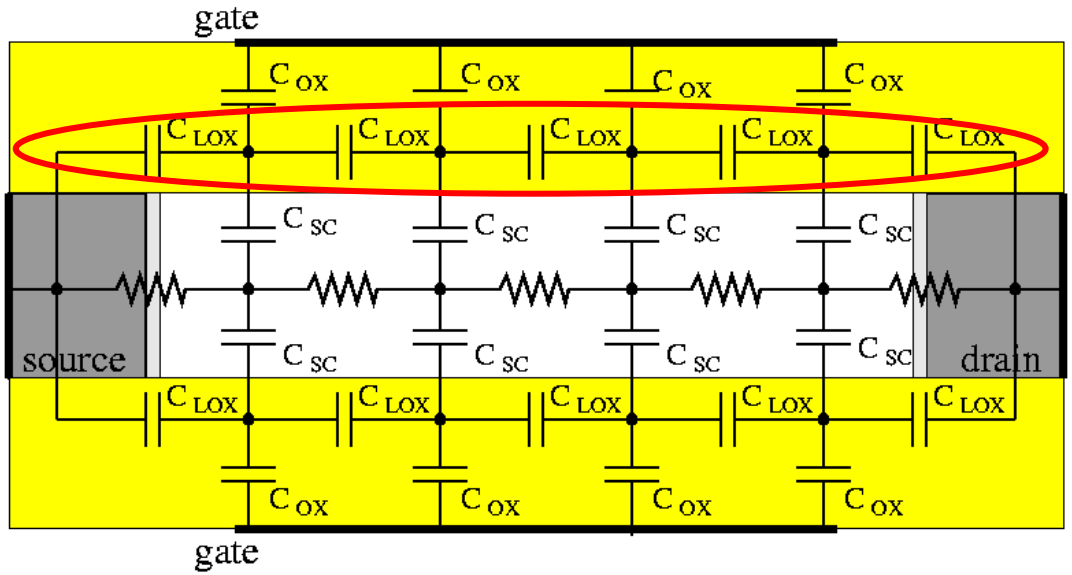
Device performance: DIBL and SS





Capacitive contribution

Both the vertical electric field in the channel and the fringing field in the oxide play a role in determining the device performance.



$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \qquad C_{ox} = \frac{2\pi\varepsilon_{ox}}{\ln\left(1+\frac{2t_{ox}}{t_{si}}\right)}$$

The lateral capacitance is expected to be given by:

$$C_{Lox} = \varepsilon_{ox} t_{ox} W/\delta$$

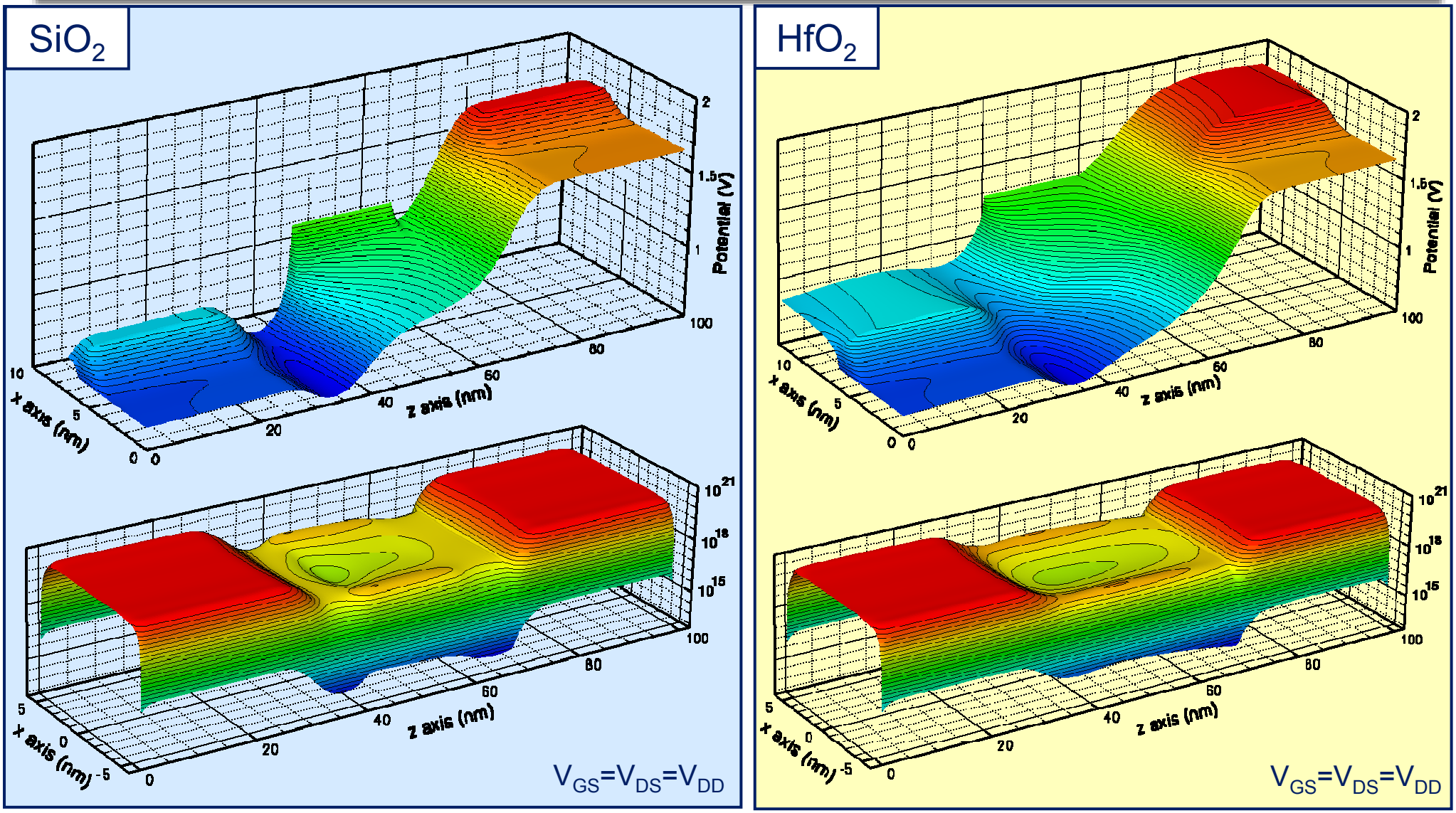
δ is the average length of the electric field lines originating from drain and ending onto the channel charge.

If HfO_2 is used at a fixed EOT:

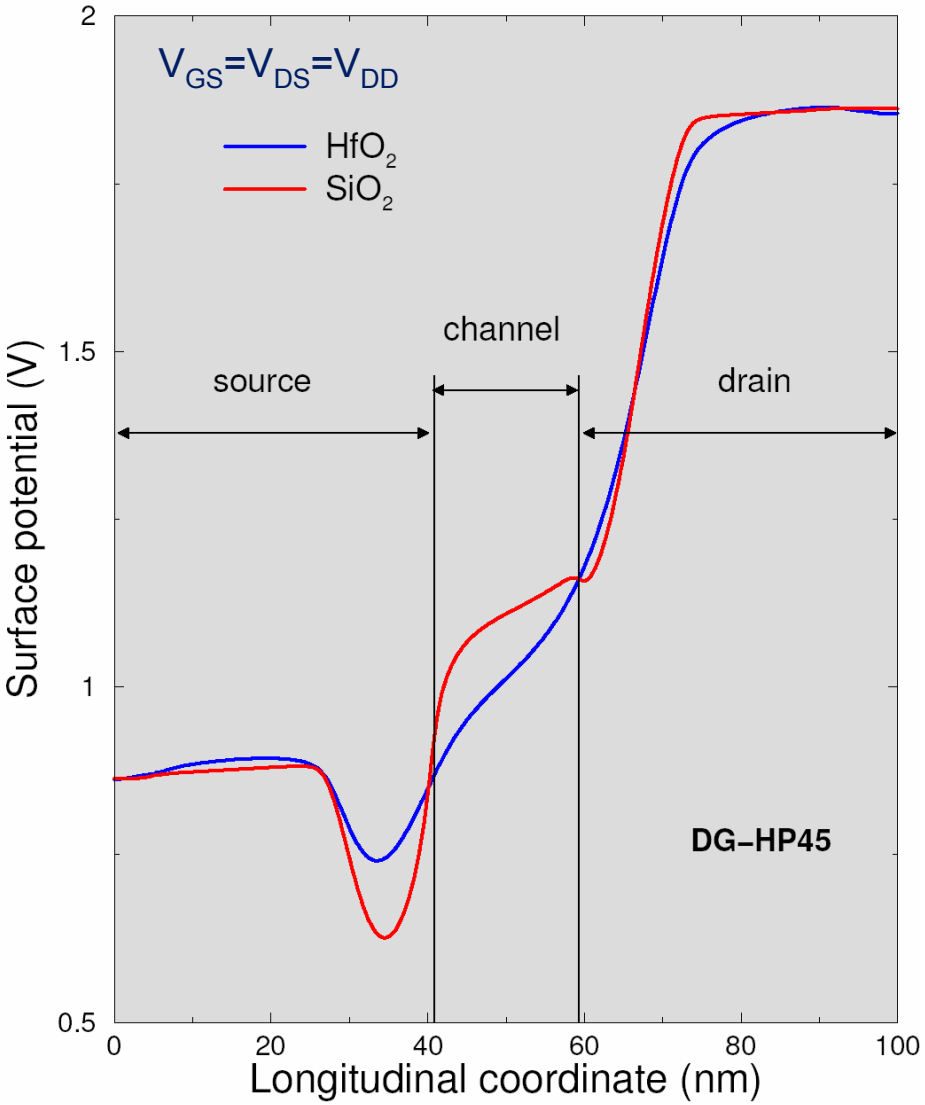
$$C_{Lox}^{HfO_2} = \lambda^2 C_{Lox}^{SiO_2}$$

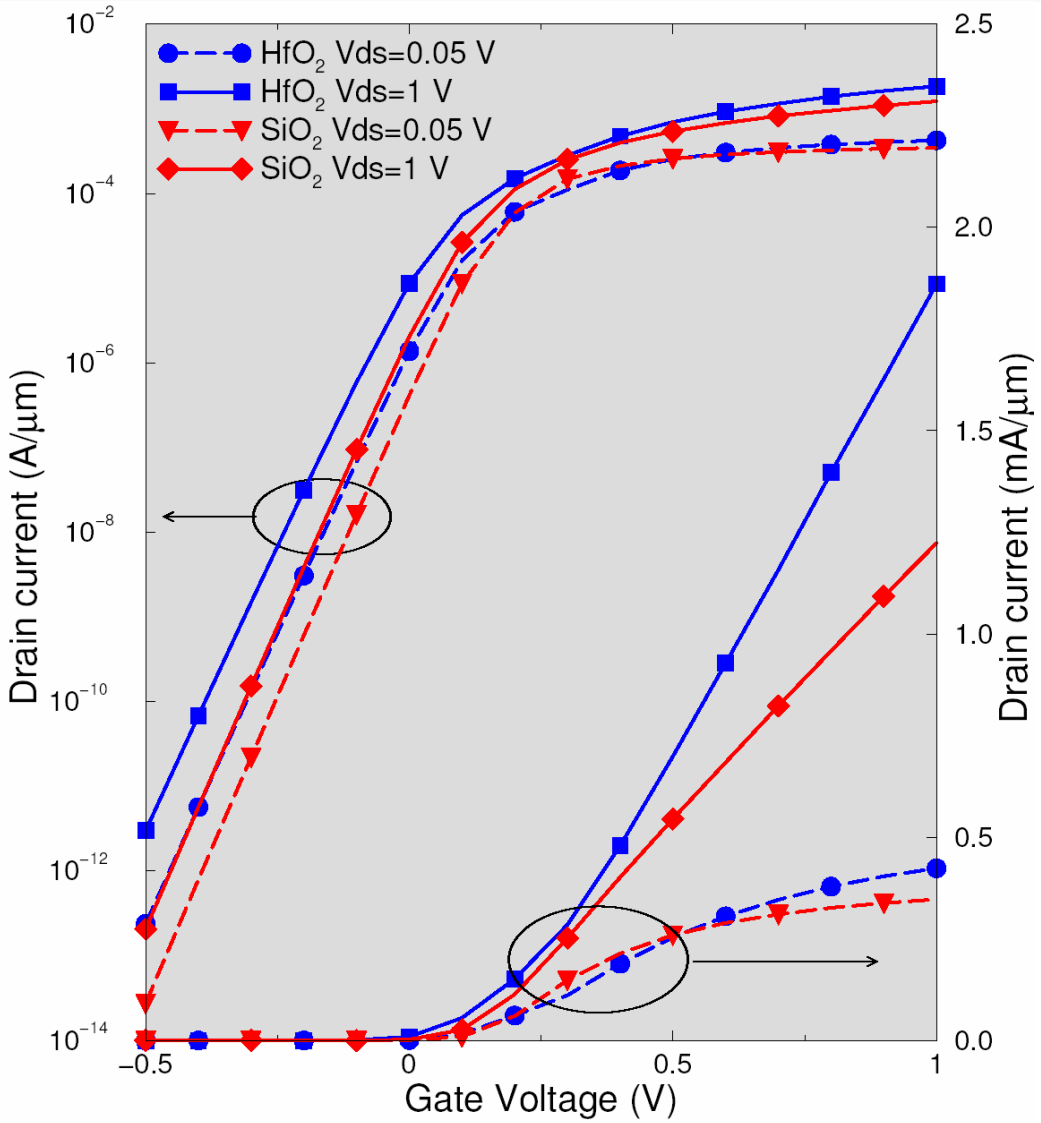
with $\lambda = k_{HfO_2}/k_{SiO_2}$

Charge distribution and potential profiles: DG HP45

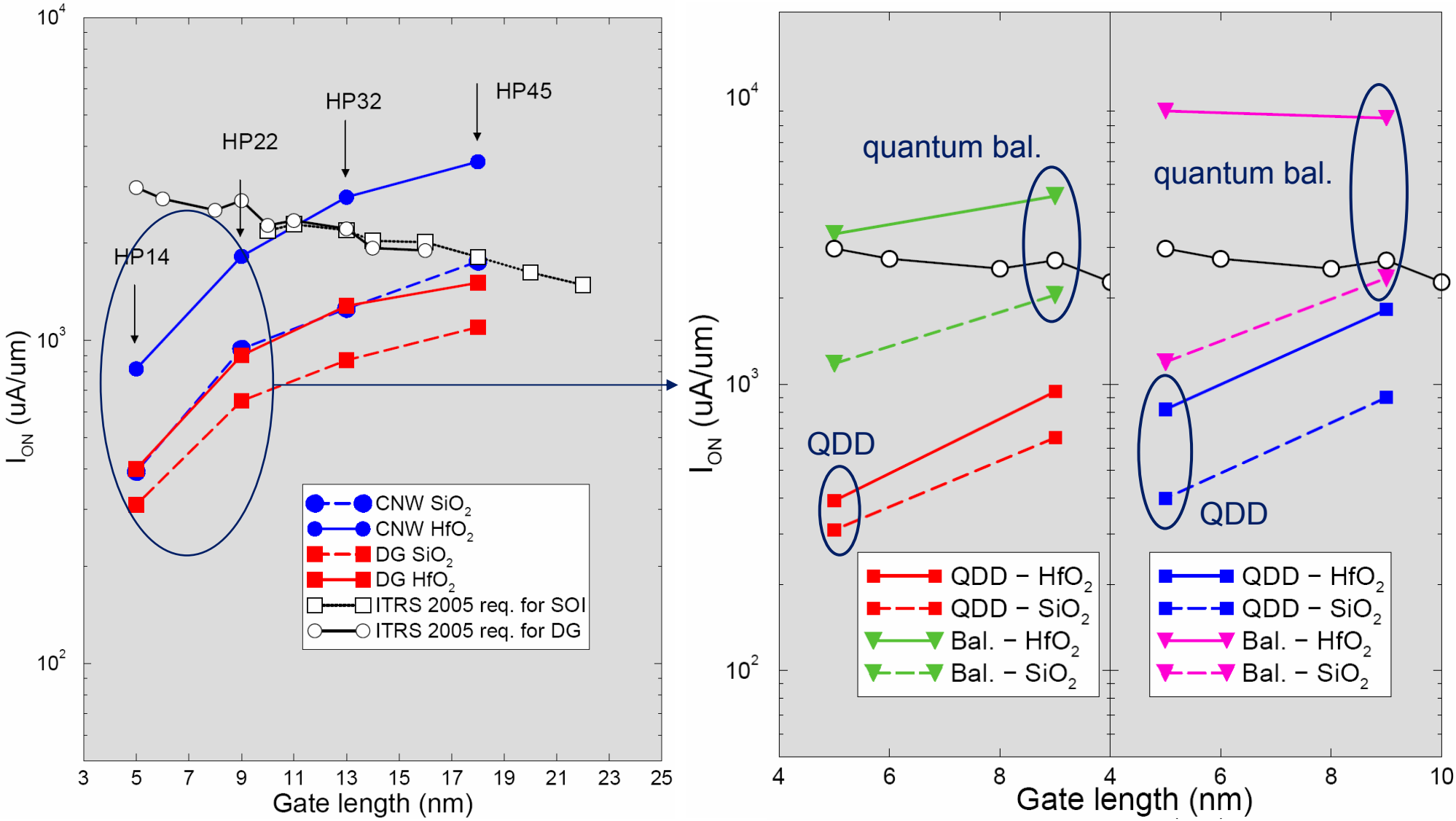


Surface potential within the channel: DG HP45





ON current vs. gate length



Outline

- Evolution from micro- to nano-electronics
- Device miniaturization and scaling theory
- Evolution of interconnects and packaging
- The ITRS and its impact on the research area
- Functional requirements of CMOS logic gates
- New device architectures
- Device modeling issues
- **Conclusions**

Conclusions

- Microelectronics has evolved to become Nanoelectronics
- Moore's law has been followed for nearly 4 decades mainly by device miniaturization
- Conventional scaling now provides diminishing returns
- New materials and new device architectures are necessary in order to comply with technology roadblocks
- Strong mobility improvements are possible by using strained channel materials, with encouraging effects on the on-current
- Device simulation requires a deeper understanding of the underlying device physics